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Dead-time analysis of digital spectrometers

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Abstract

This paper studies the impact that the outcome of new digital architectures has brought to dead time of spectrometers. Special emphasis is given to the performance comparison between conventional spectrometers and the most important architectures usually adopted in the digital solutions. Dead-time analysis is accomplished through a dedicated numerical simulation application developed with the purpose of optimizing the digital architecture performance taking into account parameters such as the incident rate of events, the existence of pulse pile-up or the complexity of the processing algorithm used during the digital pulse processing. Results of simulations using a real time multiprocessor platform (Digital Pulse Processing-M8) are presented and design options are justified accordingly.

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1. Introduction

Generally, spectrometry systems have a minimum amount of time, after a given event, during which any new incoming pulses are neglected. This limitation, usually referred to as dead time, is a direct consequence of either the physical processes in the detector medium or the timing limitations in the processing of the detected information by the associated electronics [1]. Due to the random nature of the radioactive decay process, an event can always occur very shortly after the previous one, being therefore lost for processing. These dead-time losses can be quite important at high throughput rates, so that any accurate counting system must take these losses into account and have some method to correct or minimize them.

In conventional spectrometry systems dead time behaviour is normally quite simple to model. Usually, these systems are based on well known and established architectures exclusively aiming at the determination of a very limited number of parameters from the detector's signal such as the number of incoming pulses and their amplitude distribution. Besides, the information pathway is mainly sequential in nature, i.e. the input of a given stage or functional block directly connects to the output of the previous one, and so forth. Therefore, the successive delays (latencies, conversion times, etc.) are added together resulting in the

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overall dead time of the counting system. As a consequence, most conventional systems exhibit a dead-time behaviour that can be easily described through an analytical model.

Recent developments on fast acquisition and processing technologies have induced dramatic changes in the architecture of spectrometry systems. The analog front end can now be replaced by fast high-resolution ADCs leaving all the processing burden to high-speed Very Large-Scale Integration (VLSI) devices that take care of data either by hardware Field Programmable Gate Arrays [2] or software Digital Signal Processors (DSPs) [3].

The result is a wide variety of real-time digital spectrometer architectural solutions designed and programmed according to the user specific needs. The classical in-line information pathway is now replaced by a complex digital data flow structure. In this way, dead time becomes extremely dependent on system topology characteristics as well as on design, application and operating choices. As a consequence, analytical dead-time modelling is impracticable and other dedicated tools must be used to study and evaluate the system event losses. This work presents one such tool conceived and developed with the purpose of studying the performance of digital spectrometry systems and, particularly, a scalable multiprocessor platform previously developed by the Electronics and Instrumentation Centre [4].

2. Dead-time analysis

A dedicated computational simulator was developed from scratch in C/C++ giving special attention to its versatility since the purpose of the work was to build a tool capable of easily emulating several architectures and obtaining enough characterizing data from them.

The developed software reproduces the behaviour of all the acquisition and processing chain, as well as the radioactive events by a process based on a (MC) Monte Carlo simulation. The whole process is “sample” driven rather than time driven which is typical in MC simulations. Generated “samples” can be either noise or valid events (which follow Poisson time distribution). The functions that reproduce the electronics’ behaviour include queue handlers (FIFO), countdown timers (DSP), semaphores, etc. The measured count rate is calculated by the ratio of the “processed” events to the generated ones.

This simulation allowed us to study and confirm the dead time behaviour of the main architectures usually adopted in spectrometry systems such as the conventional Multi-Channel Analyzer (MCA), or Pulse Height Analyzer, and the basic real time digital spectrometers with different memory configurations.

2.1. Conventional multichannel analyzer

The dead time of the conventional MCA is usually well described by the non-paralyzable model. This model states that a fixed amount of time τ is necessary to process each event, during which the overall system remains “blind” to new events. In the majority of the conventional MCAs, τ is mainly determined by the conversion time of the ADC added to memory transfer time and, eventually, to the extra time required for performing some linearization algorithm (e.g., the sliding scale method for differential non-linearity reduction).

Typical commercial systems have conversion times of less than 10 μs, which leads to a loss as high as 9% at 10 000 pulses/s incident rate.

2.2. Digital pulse processing architectures

In the Digital Pulse Processing (DPP) spectrometers, pulses are digitized immediately after the preamplifier stage, stored in a local sequential memory (FIFO) and then transferred to memory for real-time or off-line processing. The advantages of this architecture are well known for a long time [4]. The flexibility of the DPP approach enables, at one time, the synthesis and application of optimum weighting functions (WF) when the objective is to achieve the best possible energy resolution [5,6] and, at other time, using the same system, the application of a very simple and fast processing WF when the objective is to achieve the highest possible count rate [7]. On the other hand, the DPP approach significantly reduces the effect of the random nature of the radioactive decay process by the inclusion of several digital buffers or stacks. In fact, different DPP configurations can be adopted.

2.2.1. 1-pulse stack

In the simplest digital spectrometer architecture (Fig. 1) a memory buffer (FIFO) is placed between the acquisition and the processing blocks allowing for the storage of a new incoming pulse while the DSP is busy processing the previous one. This is called the one-pulse stack (1-PS) architecture [8].

In order to model the dead-time behaviour of a 1-PS digital spectrometer one should stress that there are two main and independent processes involved, with distinct durations: pulse acquisition (τ_1) and digitized data processing by the dedicated DSP (τ_2). During τ_1 the system is blind to new pulses while during τ_2 the digitizer and the input FIFO remain ready to receive new incoming pulses. The measured count rate m can be analytically represented as a function of the true event rate n [8]:

$$m = \frac{n}{\mathrm{e}^{-n\tau_2} + n(\tau_1 + \tau_2)}. \tag{1}$$

The measured count rate that follows this expression is represented on graph A of Fig. 3 revealing the improvement over the non-paralyzable model of a conventional MCA with dead time given by $\tau = \tau_1 + \tau_2$. This improvement will obviously be larger at low and medium incident rates and also if $\tau_2 \gg \tau_1$ as usually happens. In the example represented in Fig. 3A we have used the characteristics of the system published in Ref. [8] ($\tau_1 = 85$ µs and $\tau_2 = 640$ µs) where an improvement of about 40% is obtained at 2000 pulses per second incident rate.

2.2.2. N-pulse stack

If the memory storing ability is increased to N new pulses while the processing of the original pulse is accomplished (Fig. 2), the reduction of the dead time figure can be even more visible. This comes intuitively from the previous analysis since the second component is now related with the probability of occurrence of more than N pulses on the time interval τ_2.

This architecture can be physically implemented on a real system through the Direct Memory Access (DMA) transfer of the buffered pulses to the local processing memory of the DSP [9]. It is called an N-pulse stack architecture and its dead time behaviour is depicted on Fig. 3B for $N = 1, 2$ and 6. The throughput improvement of the system (Fig. 3C), relatively to the conventional MCA, can now reach up to 78% ($N = 6$) considering the same time intervals of the previous example ($\tau_1 = 85$ µs and $\tau_2 = 640$ µs).

This graph evidences that a larger pulse stack does not improve the dead time performance of the real time digital spectrometer at high count rates but significantly improves it at low and medium rates. This can be understood intuitively since a larger stack has a more effective derandomizing effect on the pulse processing flow (which eliminates the DSP idle times at low and medium input rates). However, if the DSP already is overloaded (as happens at high input rates), there is no margin for improvement.

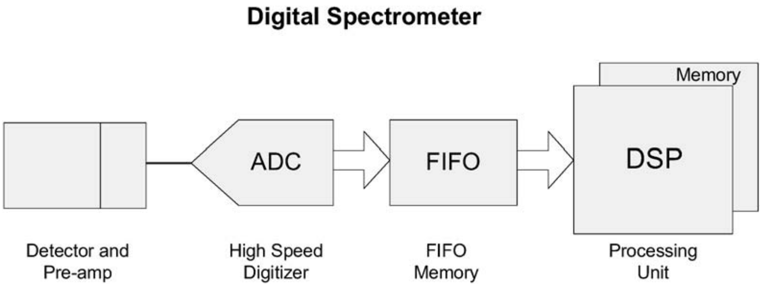

Fig. 1. Basic architecture of a Digital Spectrometer. The pre-amplified signal is digitized and stored on a local FIFO for immediate processing (real-time mode) or later treatment (off-line mode).

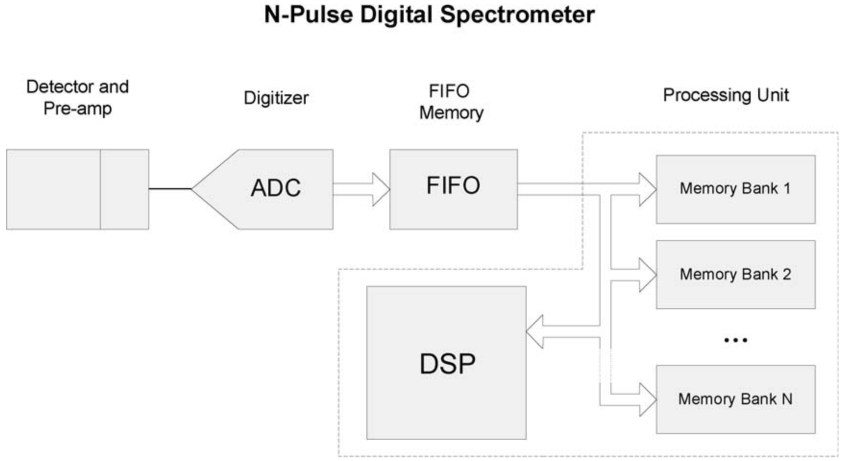

Fig. 2. Basic architecture of a Digital Spectrometer based on an *N*-pulse stack architecture. The pre-amplified signal is digitized and buffered on a local FIFO and then transferred by DMA to the next free position in the processing memory bank.

To accomplish higher throughput rates, a different approach should be made to the architecture of the digital spectrometer in order to overcome the processing bottleneck. One of the possible solutions is to increase the number of processors available for pulse processing. The system studied in the next section was designed with this aim [4] and, as we will see, the dead time analysis is of great help to determine its optimal configuration.

3. Dead-time analysis of a multiprocessor DPP system

The dead time of the configurations previously analyzed (non-paralyzable model applied to conventional MCA, 1-PS and *N*-PS DPP architectures) can be obtained analytically. However, dead time of more complex digital architectures, containing a higher degree of parallelism, is extremely difficult to assess using the conventional probabilistic approach. The best approach to analyze this kind of complex architecture is through a computational simulation tool like the one we have developed. Dead-time analysis has become such a fundamental issue in modern pulse processing architectures that it should be considered in order to correctly fit the configuration parameters of the system (depth and number of intermediate buffers and stacks, number of processing units, etc.) to the experimental conditions and user needs (input pulse rate, pile-up expectation, desired processing algorithm and throughput rate, etc.). As an example we will analyze in this section the dead-time behaviour of a multiprocessor DPP system based on eight DSPs.

The DPP-M8 is a multiprocessor digital spectrometer originally conceived for nuclear and atomic pulse spectrometry applications. It is based on a Master–Slave scalable architecture implemented with DSP. The Master Unit (MU) connects to and controls a number of peripheral interchangeable Slave Units (SUs). The main functions of the MU are to supervise the digitized pulse data transfers to the SUs, to collect the processed pulse parameters from them and to build the energy spectrum.

Also at the MU level a Trigger and Pulse Locator Unit, a Control Bus Unit and a Communication Bus interface [4] are in operation as depicted in Fig. 4.

The analog front end is similar to the one previously described, common to most digital spectrometers. It has been reduced to a linear amplifier, a trigger and pulse locator unit and a fast high-resolution digitizing block. The input signal is continuously digitized, temporarily stored

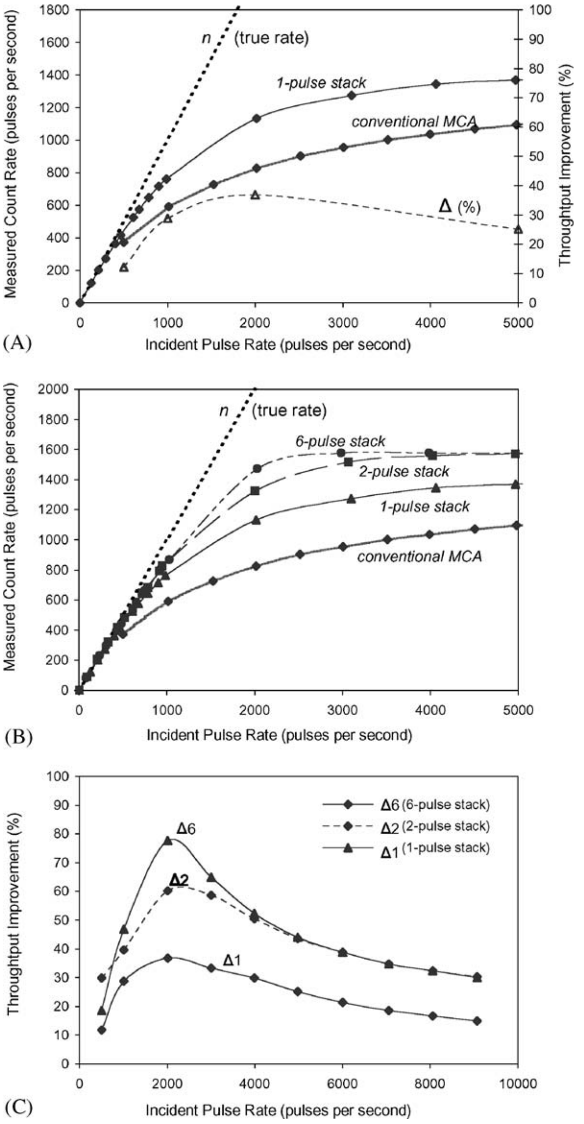

Fig. 3. Measured count rate as a function of the incident pulse rate: (A) comparison of 1-pulse stack with conventional MCA performance (Δ represents the relative throughput improvement); (B) comparison for different pulse processing stack depths (1-, 2-, and 6-pulse stack); (C) throughput improvement as a function of Pulse Stack depth. Improvement reaches 62% for 2-pulse stack (Δ2) and 78% for 6-pulse stack (Δ6).

in a FIFO and then transferred, through the pulse transfer bus, to the local FIFO of the available slave DSP. The data is processed according to the parameters established by the MU and the trigger unit.

This multiprocessor spectrometer was conceived in order to optimize the performance and count rate, minimizing the processing time usually spent to detect and prepare the pulses and, in this way, guaranteeing that almost 100% of the processing time is effectively dedicated to the application of pulse processing algorithms.

As referred, none of the analytical models of the dead time clearly reproduce the DPP-M8 behaviour. In fact, this multiprocessing architecture is based on an N-pulse stack in each SU resulting in a tree-shaped pathway for digitized data (Fig. 5). Apart from this, a series of factors account for the non-linearity of the DPP-M8 dead-time behaviour: data is transferred asynchronously to each SU FIFO according to its availability, pulse transfers to the local memory depend on its free space, DSP processing times are strongly dependent on factors such as interruptions frequency, algorithm optimization level, pulse characteristics, etc.

Under this multiprocessing architecture virtual elimination of the dead time of the system is theoretically possible, provided enough SUs are used. This can be accomplished when the following conditions are simultaneously met:

- The mean processing time spent with each pulse, divided by the number of SUs, is less than the inverse of the incident pulse rate (n).
- The space of memory allocated for temporary pulse storing is large enough to fully derandomize the pulse processing flow (eliminating the delay times and thus avoiding the consequences of the random nature of the pulse occurrence instants).

In order to determine the optimal configuration of the system (which best approximates the zero dead-time conditions), the following characteristics of the digital spectrometer can be controlled by the simulation tool:

- pulse sampling rate;
- data writing and reading clocks through the Pulse Transfer Bus;
- execution time of the pulse processing algorithm;
- number of samples used to represent each pulse;

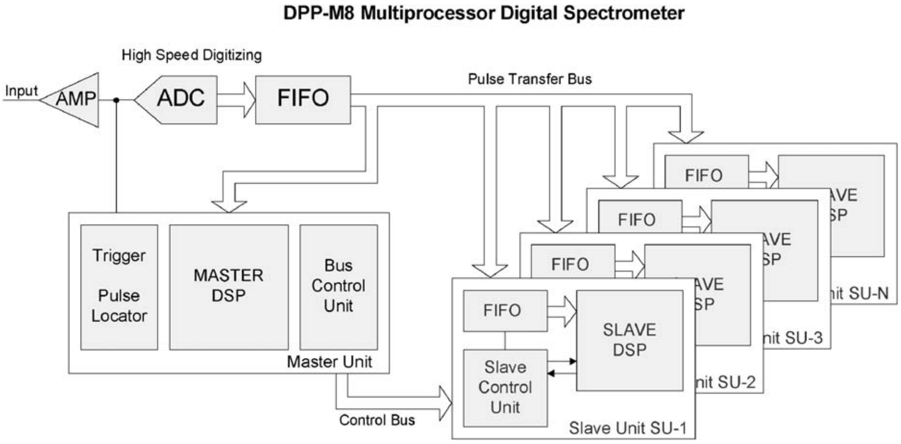

Fig. 4. Architecture of the multiprocessor DPP-M8 spectrometer. Based on a scalable Master–Slave architecture the DPP-M8 can house up to eight SUs in its basic configuration. The MU supervises the digitized pulse data transfers to the SUs, collects the processed pulse parameters from them and builds the energy spectrum (adapted from [4]).

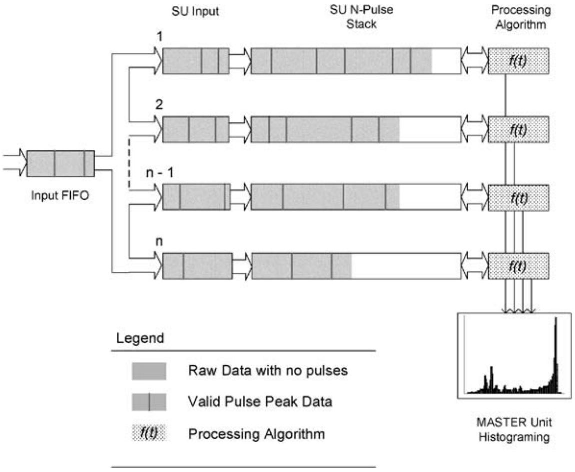

Fig. 5. Data and pulses pathway for the DPP-M8 multi-processing system. Configuration with n SUs, each containing one Input FIFO and six pulse stack ($n = 6$) buffers. Pulse steps are represented in black while ordinary data is represented in light grey.

- number of samples used to represent the weighting function;
- depth of each FIFO;
- depth and number of pulse stacks in the SUs (storing of the pulses waiting to be processed);
- number of SUs;
- behaviour of the system in face of pulse pile-up (pulse rejection or adaptive filtering).

Similarly to the case of a single N-pulse stack (Section 2), the depth of the stack plays an important role in the measured count rate of the overall system composed by several SUs. Deeper pulse stacks allow a more effective control of the DSP overloading and, as consequence, a faster convergence to the limit value (as in Fig. 3B). However, this limit value is determined only by the processing time of each pulse (630 μs in this example) turning the increase of the buffer depth almost irrelevant at high incident rates.

The simulation tool can also shed some light on the effect of using adaptive filtering as a means to overcome pile-up phenomena. This adaptive filtering consists of the detection of the pulse positions and, instead of rejecting the pulses that are not sufficiently apart from their neighbours (piled-up pulses), adapt the length of the weighting function so that only the available digitized samples are used to process that piled-up pulse [10]. This process of adaptive filtering, that can only be applied through digital methods, is extremely important in high counting rate applications.

As almost all the pulses can be processed using adaptive filtering (a dynamically configured weighting-function procedure) only the situations of extreme peak pile-up are indeed rejected, being the input count rate more closely followed until

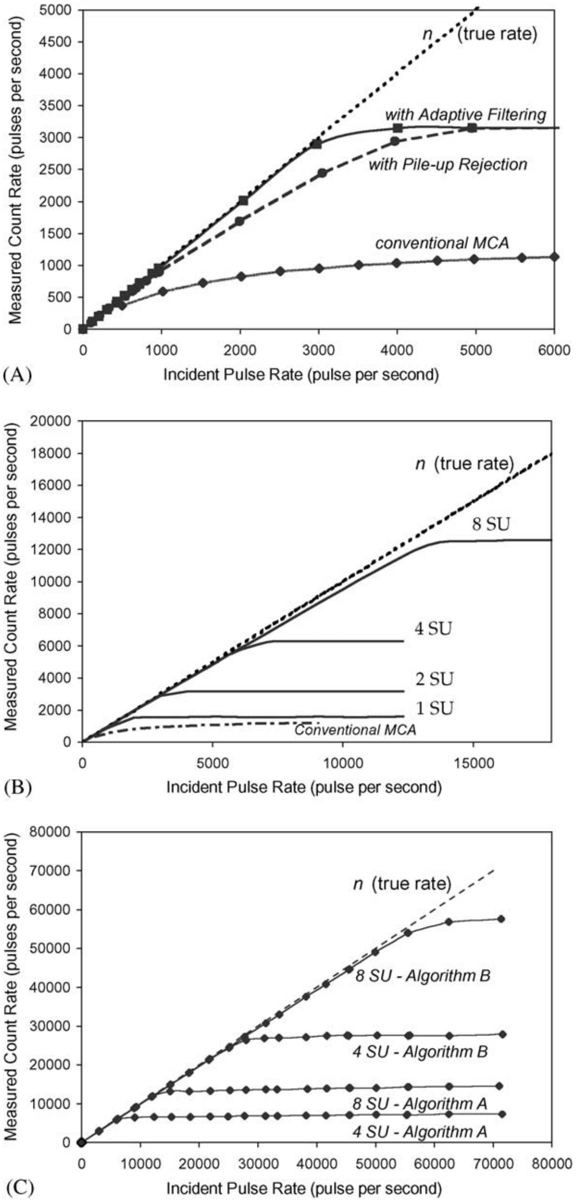

Fig. 6. Measured count rate as a function of the incident pulse rate: (A) using adaptive filtering or pile-up rejection. (System configured with two SUs each containing 6-pulse stack buffer); (B) comparative DPP-M8 throughput with 1, 2, 4 and 8 SUs, each with 6-Pulse stack buffers; (C) compromise between the measured count rate, the processing power (number of SUs) and the complexity of the processing algorithm, requiring 630 μs in the case A and 160 μs in the case B.

the saturation of the system is reached, as seen in Fig. 6A. Data in this graph have been obtained through simulation of a system with two SUs, each of them containing a 6-pulse stack processing memory buffer. As can be seen, when adaptive filter is used this configuration shows a throughput that is almost equal to the input rate until the limit of the system is reached.

Another important feature is the linear dependence of the system throughput on the number of SUs used in the multiprocessor configuration (Fig. 6B). The 1600 pulses/s plateau obtained with a single SU is doubled when using two SUs and reaches 12 800 pulses/s when using the maximum processing capacity of eight SUs. The slight deviation between the measured count rate and the incident rate of events is due to peak pile-up rejection.

Finally, the compromise between the count rate, the processing power (i.e. the number of SUs) and the complexity of the processing algorithm becomes evident in Fig. 6C where we compare the performance of the system with four and eight SUs using two algorithms requiring different processing times (the one considered so far that executes in 630 μs and a simpler one with 160 μs of execution time).

The application of the developed simulation tool to this multiprocessor DPP architecture allowed us to obtain important conclusions concerning its ideal configuration. For instance, it was verified that a 6-pulse stack for each SU is enough in order to guarantee a constant pulse processing regime. It was also verified that, in order to reach a throughput of 10^3 pulses per second, eight SUs have to be used if algorithm A is required. However, for applications that can make use of algorithm B (or if four times faster DSPs are available) two SUs would be enough to obtain the same overall throughput. It is important to state that these data were obtained under identical clock speeds for the ADC, the input FIFO and the writing and reading cycles on the Pulse Transfer Bus as well as 512 samples (corresponding to 10 μs) to represent each pulse. Different conclusions might be obtained in different circumstances which reveals the importance of this tool and this kind of analysis in order to optimize the configuration of a DPP system as complex as this one.

4. Conclusions

The dead time of typical spectrometer configurations (non-paralyzable model applied to conventional MCA, 1-PS and *N*-PS DPP architectures) was analysed and analytically obtained. However, the dead time of more complex digital architectures, containing higher degree of parallelism, was considered to be extremely difficult to determine using the conventional probabilistic approach. Therefore, the best approach to analysing this kind of complex architecture is through a computational simulation tool like the one developed. It was shown that dead-time analysis should be considered in order to adapt the configuration of the digital system (depth and number of intermediate buffers and stacks, number of processing units, etc.) to the experimental conditions and user needs (input pulse rate, possibility of pile-up occurrence, desired processing algorithm and throughput rate, etc.) and conclusions were obtained regarding a multiprocessing architecture based on up to eight DSPs.

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