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Finite Control Set Model Predictive Control for Paralleled Uninterruptible Power Supplies

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Abstract: Nowadays, uninterruptible power supplies (UPS) play an important role in feeding critical loads in the electric power systems such as data centers or large communication hubs. Due to the increasing power of these loads and frequent need for expansion or redundancy, UPS systems are frequently connected in parallel. However, when UPS systems are parallel-connected, two fundamental requirements must be verified: potential circulating currents between the systems must be eliminated and the load power must be distributed between the systems according to UPS systems availability. Moreover, a high-quality load voltage waveform must be permanently ensured. In this paper innovative control strategies are proposed for paralleled UPS systems based on Finite Control Set Model Predictive Control (FCS-MPC). The proposed strategies simultaneously provide: controlled load power distribution, circulating current suppression and a high-quality load voltage waveform. A new dynamic converters deactivation mechanism is proposed. This new technique provides improved overall system efficiency and reduced power switches stress. In this paper, two multilevel based UPS systems are parallel-connected. Each UPS contains two three-level Neutral Point-Clamped-Converters (3LNPC) and a three-level DC-DC converter. The presented experimental results demonstrate the effectiveness of the proposed control strategies in several operating conditions.

Keywords: model predictive control; uninterruptible power supplies; multilevel converters; power quality

1. Introduction

Uninterruptible Power Supplies (UPS) are used to feed a wide range of electrical loads: from low-power applications (such as domestic computers and networks) to high-power applications of several Megawatt (such as data centers and medical facilities). Over the years, with the emergence of high-power, more important and sensitive critical loads, two main reasons have motivated the connection of UPS systems in parallel: power capacity expansion and improved redundancy [1–3].

Usually, when a UPS is installed in a facility, it has a fixed nominal power. However, if more critical loads are installed in this facility, the required power may exceed the power that the installed UPS is able to supply. In this situation, instead of replacing the installed UPS by another with higher nominal power, a second UPS can be installed in parallel with the existing one.

Despite the reliability typically provided by a UPS system, there is always the possibility of intrinsic system failures such as semiconductor and passive element (input and output filters) faults. For certain types of critical loads such as high-tier data centers, very high redundancy levels are required. Those redundancy levels are typically achieved by connecting several UPS modules in parallel. In this case, when a UPS system fails, the other redundant systems can continue supplying the

load. Due to the fact that maintenance is required in all UPS systems, it is also of prompt importance to have more than just one installed UPS system. The connection of several UPS systems allows the disconnection of a given UPS to perform maintenance actions on it, while the remaining modules continue feeding the load.

When UPS systems are parallel-connected, two fundamental requirements must be verified: potential circulating currents between the systems must be eliminated and the load power distribution must be fully controlled. Moreover, a high-quality load voltage waveform must be permanently ensured.

In a parallel connection, the inputs/outputs of each system are connected to the same physical points. Thus, closed paths are formed leading to the circulation of an undesired current between the paralleled modules. This circulating current is not an exclusive problem to the parallel of UPS modules. Actually, the dynamics of this current has been extensively studied in the scope of the paralleled DC/AC converters [4,5]. This current is commonly defined as Zero Sequence Circulating Current (ZSCC). The ZSCC causes additional power losses in the overall system and inhibits a precise load-sharing between the paralleled systems. It can even increase the phase currents to hazardous values, triggering overcurrent protections. Thus to ensure a stable operation of any kind of paralleled power converters, this current must be effectively suppressed. However, in the scope of paralleled full UPS modules, the dynamics of this current has not yet been studied.

Another important functionality in paralleled UPS systems is the ability to control the load power distribution between the modules. Most proposed controllers for paralleled systems ensure an even power distribution between the modules, ensuring equal stress and usage/losses in the various modules. However, an asymmetric load power distribution can have enormous advantages. The efficiency of a power conversion system typically increases with increasing load. When a system operates at low power load, power losses become more significant, typically leading to low efficiency values. Therefore, in paralleled converters, an asymmetric power distribution can increase the overall system efficiency. Moreover, if one system is not able to supply its power target (for example, due to a fault), the other systems must increase their target power, to maintain a correct system operation (but the faulty module can still provide a lower power, instead of being completely deactivated). This can only be achieved through a fully controlled load-power distribution [6].

Control strategies that ensure equal load current distribution between paralleled UPS systems have been proposed in the literature. According to [1,2], these strategies can be divided into two distinct groups, depending on the presence of intercommunication between the paralleled UPS controllers (Figure 1). If the controllers of each UPS share information, the control scheme is defined as *active load-sharing* scheme. Otherwise, if no communication is required between the controllers, the control scheme is classified as *independent* scheme.

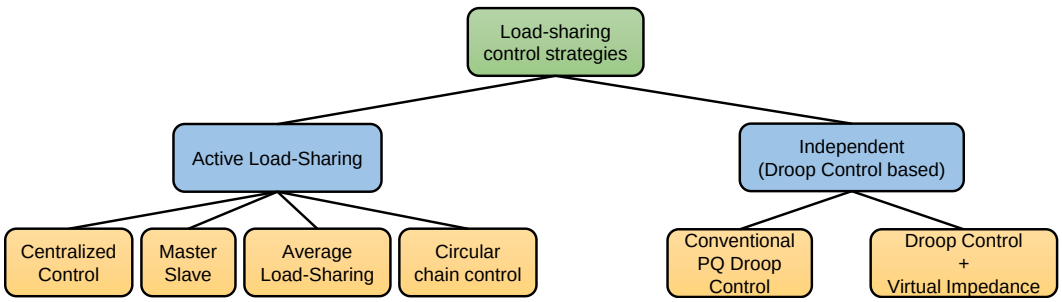

Figure 1. Main types of load-sharing control schemes used for paralleled connected UPS (adapted from [1,2]).

Active load-sharing methods are classified into four distinct groups: centralized, master–slave, average load-sharing and circular chain control methods. In a centralized control scheme, the load voltage and the total load current are measured and sent to a centralized controller that generates

a current reference. This current is divided by the number of paralleled systems and sent to their respective controllers [7,8]. In a Master–slave control scheme, the Master controller uses a voltage control loop to regulate the load voltage by generating a current reference for its own (having into account the number of paralleled units). The current that the master is supplying to the load is used as the same reference for the slave modules [9–11]. In the average load-sharing schemes, the voltage reference is generated inside each UPS controller. All output currents are measured. An average current value is computed, and each UPS controller must track the computed average value [3,12,13]. In a circular chain control scheme, the current reference for the first UPS is directly obtained from the measurement of the current of last UPS system and so on, creating a circular chain connection [14–16].

In the independent control schemes, by controlling the amplitude and phase difference between the inverter voltage and load voltage, the reactive and active power supplied by each paralleled system is controlled (conventional PQ droop control). However, a conventional PQ control scheme has poor performance for non inductive loads [17,18]. Hence, strategies consisting of the conventional droop method with an additional virtual impedance loop have been proposed [19–21]. In independent control strategies, since the load voltage references are controlled to achieve load-sharing, a tradeoff between a precise load power distribution and a high-quality load voltage waveform typically exists.

Regardless of the used control strategy, each UPS is typically controlled by a dedicated control platform. As mentioned above, different control principles may or may not require communication between control platforms. Techniques based on droop control, do not require communication between platforms and are therefore easily applicable to multiple paralleled systems. On the other hand, active load-sharing techniques provide improved performance but require real-time communication between the controllers. This poses a technical difficulty, which may limit the applicability of the solutions, or increase their cost, if more advanced control platforms or additional components are needed. This difficulty is highly dependent on the amount of data to be transferred between controllers and the timing of this data transfer.

In order to avoid the disadvantages of droop control, active load-sharing techniques have to be used. However, these require real-time communication between the controllers which may be a significant problem when working with control techniques with very high complexity and low sampling times, as is the case of FCS-MPC. In most active load-sharing techniques, the references to be followed by each UPS are calculated and then need to be transmitted to its respective controller [9–11]. This means that each controller needs to wait for this information to arrive in order to continue computing the control scheme. Hence, part of the period available to perform the required calculations is wasted waiting for this information, which can be critical for FCS-MPC solutions.

In this paper, an active load-sharing FCS-MPC technique is proposed with low real-time communication requirements, thus providing excellent performance, without compromising the industrial feasibility of the technique. In the proposed control strategy just the current of each DC/AC converter and the Common Mode Voltages (CMV) generated by each UPS (to improve ZSCC suppression capabilities of controllers) are shared between UPS controllers. Since CMV values correspond to signals from the previous sampling time, the communication of these signals can start before the current sampling. On the other hand, since the converter currents are measured directly and do not require any additional processing or calculations, they can be transmitted immediately after sampling. This means the required communication should not pose a significant delay to the computation of the control algorithm.

When compared to more conventional control strategies, Finite Control Set Model Predictive Control (FCS-MPC) allows an easy inclusion of system non-linearities and hard constraints. This control approach provides also higher steady-state performance and faster transient response [22,23] and have proven to be a very promising solution for UPS systems [23,24]. Several FCS-MPC based strategies have also been proposed for several other applications that do not require a high number of converters or a strict cooperation between them, such as standalone rectifiers [25], drives [26,27], static synchronous

compensators (STATCOM) [28,29] and grid-connected DC/AC converters [4,5,30,31]. However, relatively few studies have been proposed for multi-converter systems using FCS-MPC.

The faster transient response provided by FCS-MPC compared to more conventional control techniques makes FCS-MPC a very promising control strategy to be used in paralleled UPS systems [6,23]. For example, when a UPS system is not able to supply its power target, the power target of the other systems must be quickly increased, to ensure that the critical load is correctly fed. More conventional control strategies will face several limitations in this topic. Moreover, the high cooperative principle enabled by FCS-MPC in a complex multi-converter system, such as the one studied in this paper, allows the control action computed for some converters to be considered when choosing the control action of other converters [6,23,32] which can lead to improved overall system performance. This turns FCS-MPC into a technique with enormous potential for example to eliminate the undesired circulating currents that flow between paralleled UPS systems [6,32].

This very promising cooperation principle has been scarcely explored in the literature not only in the scope of paralleled UPS systems but also for other complex multi-converter systems. In [23], a cooperative strategy is proposed but just for a standalone UPS system. In the field of paralleled UPS systems, two cooperative based strategies are proposed in [6,32], however in both of these studies the DC/DC converters and respective battery banks were not considered in both paralleled UPS. In [33] a FCS-MPC strategy is proposed for paralleled UPS systems, however it merely addresses the operation of the DC/AC converters in which no circulating current problems exist, which significantly simplifies the required control design. Moreover, in this study the load voltage references are generated based on a droop control scheme, which for some types of loads may represent a tradeoff between a precise load-sharing and a high-quality load voltage waveform.

Given all these facts, a cooperative-based FCS-MPC strategy that considers not only the cooperation potential between the converters within a UPS but also between the converters of both UPS systems, is proposed in this paper to control all converters of two complete paralleled UPS systems based on a multilevel topology. Each UPS contains a three-level DC-DC, in addition to two three-level Neutral-Point-Clamped (3LNPC) converters. Multilevel converters have a lot of advantages when compared to the conventional two-level converters [34], such as lower voltage applied to each power switch with the same DC bus voltage and lower current waveform distortion. The three-level Neutral Point Clamped converter has been the object of intense research in the last few decades as well as its use in Back-to-Back (BTB) [35,36] and UPS topologies [6,23,32].

Several limitations can be observed in most studies found in the literature regarding paralleled UPS systems. First, the used UPS configurations are based on conventional two-level power electronics converters. Second, with the exception of [10], the paralleled systems are typically symmetric (same electrical components and power ratings). In the available studies the load power is equally divided by the paralleled systems which inhibits the aforementioned asymmetric load-sharing advantages. Moreover, the dynamics of the circulating currents in paralleled UPS system as well as strategies for its suppression are still not defined since in the major part of the proposed studies, merely the DC/AC converters operation is studied. The major part of available studies uses more conventional control strategies such as linear ones (e.g., PI with PWM). Finally, no dynamic mechanism for the activation/deactivation of power converters according to the different operation modes is yet proposed for paralleled UPS systems.

In this paper a cooperative-based FCS-MPC control strategy that simultaneously ensures high load-sharing precision, high-quality load voltage waveforms and ZSCC suppression is proposed. The proposed strategy is validated for extensive operating conditions, demonstrating the potential and effectiveness of FCS-MPC for complete multilevel paralleled UPS systems. To demonstrate that the proposed control strategy can operate correctly even with asymmetric paralleled UPS systems, different filter parameters were used in the two UPS systems used in the experimental tests. A control scheme based on FCS-MPC is proposed for the paralleled systems that allows a fully controlled power distribution (symmetric or asymmetric) and an effective ZSSC elimination. The possibility to obtain a

fully controlled asymmetric power distribution can be highly advantageous, because it allows modules with different power ratings to be correctly connected in parallel and enables efficiency and reliability improvement techniques to be implemented. The system efficiency in different modes of operation is also studied, namely for normal (grid available) and stored energy (grid unavailable) operation modes. For these two operation modes a converters deactivation mechanism is proposed ensuring improved system efficiency and reduced stress in converters' power switches. The experimental results demonstrate that even for asymmetric paralleled systems, the proposed control strategies simultaneously ensure at any operating condition: a perfectly controlled load power distribution, circulating current suppression and a high-quality load voltage waveform. The effectiveness and advantages of the proposed converters deactivation mechanism is also demonstrated.

This paper is organized as follows: in Section 2, the mathematical model of the UPS systems and the dynamics of ZSCC are presented. The discretized model equations and the principles of Finite Control Set Model Predictive Control (FCS-MPC) are demonstrated in Section 3. In Section 4, the experimental results are presented and discussed. Section 5 concludes the paper.

2. Mathematical Model

The detailed circuit configuration of the adopted system is presented in Figure 2. The measured signals are represented in red. Each UPS system contains a grid-side converter (GSC), a DC-DC converter (DCC) and a load-side converter (LSC) that share a double-capacitor DC bus. Each GSC is connected to the grid using an inductive filter while each LSCs is connected to the load through an LC filter. Each DC-DC converter is connected to the respective battery bank through and inductive filter.

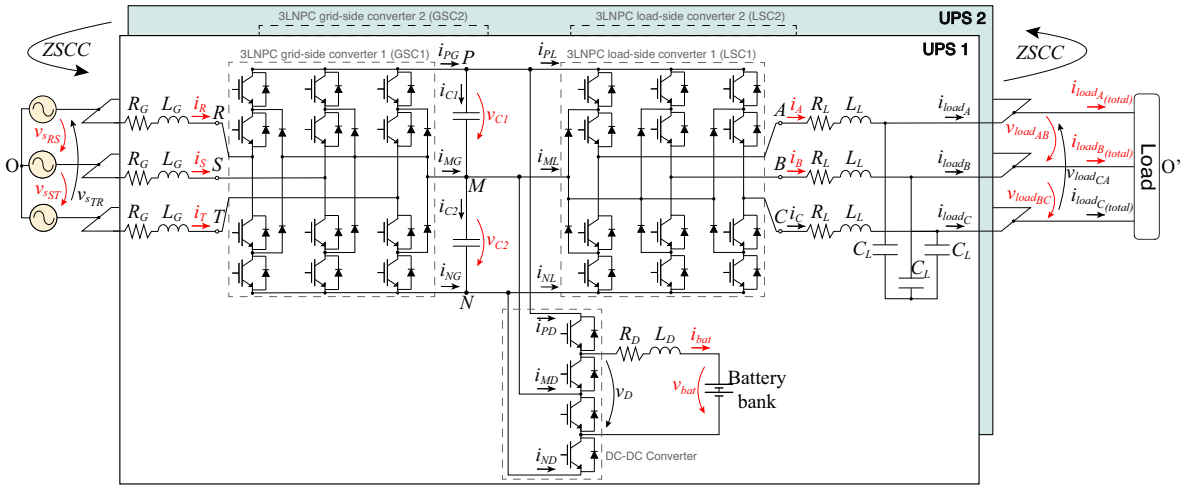

Figure 2. Circuit diagram of the proposed paralleled system.

Regarding the GSCs and the LSCs, the adopted 3LNPC topology contains three legs, each of them associated to a given phase X. For the GSC $X = \{R, S, T\}$, whereas for the LSC $X = \{A, B, C\}$. Each leg contains four IGBTs (with anti-parallel diodes) and two clamping diodes. For each phase there are three distinct switching states, leading to three different pole voltage (v_{XM}) values, as shown in Table 1.

Table 1. GSC/LSC switching states in phase X.

GSC/LSC Switching State (S_X)	Active IGBTs	Generated Pole Voltage (v_{XM})
1	Upper two	v_{C1}
0	Middle two	0
-1	Lower two	$-v_{C2}$

The pole voltage corresponds to the voltage between the AC terminal of phase X and the middle point M of the DC bus. Therefore, each 3LNPC converter has 27 possible switching states. Usually, to simplify the control of a converter, three-phase variables are transformed to space vector form. Regarding the GSC, such transformation is given by

$$\overline{x} = \frac{2}{3}(x_R + ax_S + a^2 x_T) = x_\alpha + jx_\beta \,, \tag{1}$$

where $a = e^{j\frac{2\pi}{3}}$ represents the space rotation coefficient and $\overline{x}$ represents the space vector. The LSC variables are transformed analogously.

The DC-DC converter consists of a three-level leg with no clamping diodes. As represented in Table 2, four different switching states can be applied to the converter.

Table 2. DC-DC converter switching state.

DCC Switching State (S_D)	Active IGBTs (Top to Bottom)	Converter Voltage (v_D)
0	Two and Three	0
1	One and Three	v_{C1}
2	Two and Four	v_{C2}
3	One and Four	v_{DC}

2.1. Grid-Side Converter

The mathematical model of each GSC is now defined. From Figure 2 the following voltage equation can be written

$$v_{s_X} = L_G \frac{di_X}{dt} + R_G i_X + v_{XM} - v_{OM} \,. \tag{2}$$

The term v_{s_X} corresponds to the grid phase voltage which is calculated from the measured line voltages. The term i_X corresponds to the grid current. The term v_{OM} corresponds to the converter Common Mode Voltage (CMV). The O point corresponds to the neutral grid point. The CMV is deduced from (2), and is given by

$$v_{OM} = \frac{v_{RM} + v_{SM} + v_{TM}}{3} \,. \tag{3}$$

All three-phase signals are transformed to vector form. This removes the CMV component, simplifying the converter control. Therefore, (2) can be rewritten as

$$\overline{v}_s = L_g \frac{d\overline{i}_g}{dt} + R_g \overline{i}_g + \overline{v}_g \,. \tag{4}$$

where $\overline{v}_s$ is the grid voltage space vector, $\overline{i}_g$ is the grid current space vector and $\overline{v}_g$ is the converter voltage space vector. From (4), the dynamics of the grid-side current is given by

$$\frac{d\overline{i}_g}{dt} = \frac{\overline{v}_s}{L_g} - \frac{R_g}{L_g}\overline{i}_g - \frac{\overline{v}_g}{L_g} \,. \tag{5}$$

The dynamics of DC bus capacitors voltage are defined as

$$\frac{dv_{C_n}}{dt} = \frac{1}{C_{DC}} i_{C_n} \,, \quad n = \{1, 2\} \,, \tag{6}$$

where the currents in the DC bus capacitors are given by

$$i_{C1} = i_{P_G} - i_{P_L} - i_{P_D} \,, \tag{7}$$

$$i_{C2} = -i_{N_G} + i_{N_L} + i_{N_D} \,. \tag{8}$$

In these equations, i_{P_G} and i_{N_G} are the currents supplied to the DC bus by the GSC, whereas i_{P_L} and i_{N_L} are the currents absorbed by the LSC. The i_{P_D} and i_{N_D} terms correspond to the currents absorbed by the DCC. The capacitance of each DC bus capacitor is the same and is given by the term C_{DC}. The currents absorbed by the DC bus are given by

$$\begin{aligned} i_{P_G} &= i_R\,(S_R = 1) + i_S\,(S_S = 1) + i_T\,(S_T = 1) \\ i_{M_G} &= i_R\,(S_R = 0) + i_S\,(S_S = 0) + i_T\,(S_T = 0) \\ i_{N_G} &= i_R\,(S_R = -1) + i_S\,(S_S = -1) + i_T\,(S_T = -1)\,, \end{aligned} \tag{9}$$

where $(S_X = s)$ is 1 if S_X has value s and 0 otherwise. The currents i_{P_L}, i_{M_L}, i_{N_L} are obtained analogously. The currents i_{P_D}, i_{M_D}, i_{N_D} are defined in Section 2.3.

2.2. Load-Side Converter

Similarly to the mathematical model deduction made for each GSC in the previous subsection, the LSC mathematical model is now presented. The following phase voltage equation can be written

$$v_{load_X} = -L_L \frac{di_X}{dt} - R_L i_X + v_{XM} - v_{O'M}\,, \tag{10}$$

where the term v_{load_X} is the load phase voltage which is calculated from the measured line voltages. The term i_X corresponds to the LSC output current. The terms v_{XM} and $v_{O'M}$ are respectively the pole voltage and CMV of the LSC, being O' in this case a fictitious neutral load point. The current i_X is given by

$$i_X = i_{load_X} + i_{C_{L_X}} = i_{load_X} + C_L \frac{dv_{load_X}}{dt}\,. \tag{11}$$

In vector form, (10) and (11) are given respectively by

$$\overline{v}_{load} = -L_L \frac{d\bar{i}_L}{dt} - R_L \bar{i}_L + \overline{v}_L\,, \tag{12}$$

$$\bar{i}_L = \bar{i}_{load} + C_L \frac{d\overline{v}_{load}}{dt}\,. \tag{13}$$

Hence, the voltage and current dynamics are given by

$$\frac{d\bar{i}_L}{dt} = -\frac{1}{L_L}\overline{v}_{load} - \frac{R_L}{L_L}\bar{i}_L + \frac{1}{L_L}\overline{v}_L\,, \tag{14}$$

$$\frac{d\overline{v}_{load}}{dt} = \frac{1}{C_L}\bar{i}_L - \frac{1}{C_L}\bar{i}_{load} \tag{15}$$

2.3. DC-DC Converter

Regarding the DCC, from Figure 2 the following voltage equation is obtained

$$v_{bat} = v_D - L_D \frac{di_{bat}}{dt} - R_D i_{bat}. \tag{16}$$

From Equation (16) the dynamics of the battery current is given by

$$\frac{di_{bat}}{dt} = -\frac{R_D}{L_D} i_{bat} - \frac{1}{L_D} v_{bat} + \frac{1}{L_D} v_D. \tag{17}$$

The currents drawn/supplied from the DC bus by the converter are given by

$$\begin{aligned} i_{P_D} &= i_{bat}\left((S_D = 1) + (S_D = 3)\right) , \\ i_{M_D} &= -i_{bat}\,(S_D = 1) + i_{bat}(S_D = 2) , \\ i_{N_D} &= -i_{bat}\left((S_D = 2) + (S_D = 3)\right) , \end{aligned} \tag{18}$$

where $(S_D = n)$ is 1 only if $S_D = n$, otherwise this term is considered 0.

2.4. Circulating Current Analysis

In this subsection an analysis regarding the generation of the circulating current is made. The DC-DC converters and the battery banks have no influence on the circulating current dynamics. Hence, these components are overlooked in this analysis, as shown in Figure 3.

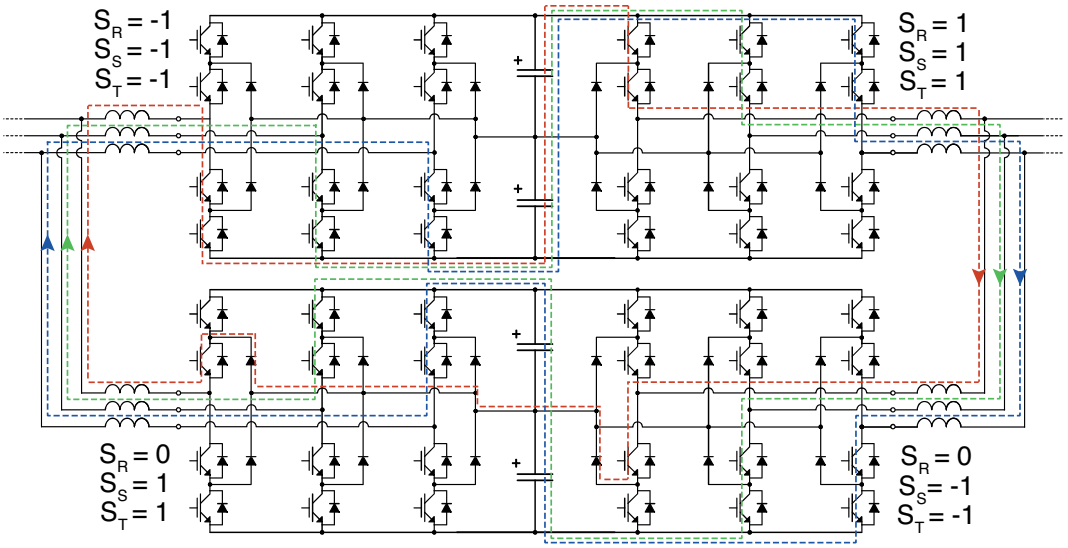

Figure 3. Circulating current generation example.

In a three-phase three-wire system, the sum of the phase currents is always zero. This is valid in the case in which a single three-wire UPS supplies a critical load. However, when two or more UPSs are connected in parallel, internal closed paths are formed according to the different switching states applied to the converters of the two systems. When different switching states are applied in the converters of different UPS systems, a high voltage (from the DC buses) is applied to the inductive filters, generating a circulating current. Figure 3 shows an arbitrary moment during the system operation in which a circulating current is being formed. All the converters have different switching states applied. It can be seen that the voltage sources that create these currents are the DC buses of each UPS. The circulating current in phase *R* (represented in red) is during the given switching states only generated by the DC bus of UPS1, whereby in the phase *S* and phase *T* (represented in green and blue, respectively), the circulating current is generated by the voltages of the two DC buses (note that due to the converters switching states applied in phase *S* and *T* the DC buses are in series from the point of view of these phases). Since the high voltages of the DC buses are only applied to the inductors of the grid and load side filters, very low impedance paths are formed, leading to high circulating currents. Therefore, the circulating current dynamics depends on the voltages of the DC buses, switching states of the converters (which can be quantified as the CMV generated by each converter as it will be seen bellow) and on the impedance of the filters.

As it was seen, the current of each phase may have a common DC current component, generating a zero-sequence current component. Therefore, in general, the literature designates the circulating current that exists in a paralleled power electronics system as a zero sequence circulating current (ZSCC). From the point of view of a UPS system controller, the ZSCC that circulates between the UPS

systems through the connection points, can be detected by adding the phase currents at any point of the paralleled system.

To obtain this current, instead of only two currents, all three grid currents of each UPS are measured. The ZSCC is given by

$$i_0 = \frac{i_R + i_S + i_T}{3} . \tag{19}$$

Similarly to the ZSCC dynamics analysis given in [4] for the parallel connection of two three-level DC/AC converters, the dynamics of the ZSCC for the proposed paralleled system is deduced and given by:

$$\frac{di_0}{dt} = \frac{(v_{OM_{G2}} - v_{O'M_{L2}} + v_{O'M_{L1}} - v_{OM_{G1}}) - i_0 \cdot (R_{G_1} + R_{L_1} + R_{G_2} + R_{L_2})}{(L_{G_1} + L_{L_1} + L_{G_2} + L_{L_2})} . \tag{20}$$

where the terms $v_{OM_{G2}}$, $v_{O'M_{L2}}$, $v_{O'M_{L1}}$, $v_{OM_{G1}}$ are the CMV of each converter, calculated using (3), and R_{G_1}, R_{G_2}, R_{L_1}, R_{L_2} and L_{G_1}, L_{G_2}, L_{L_1}, L_{L_2} are the grid-side and load-side filter resistances and inductances of both UPS systems. Hereafter, the subscripts 1 and 2 will be used in mathematical model and control description to distinguish terms referring to UPS1 and UPS2, respectively. The chosen convention for the positive direction of ZSCC is depicted in Figure 2. From (20) it can be seen that ZSCC dynamics highly depends on the linear combination of CMV of all the converters. Thus, by controlling the CMV generated by the converters, the ZSCC can be controlled.

3. Proposed FCS-MPC Controller

The control scheme explained in this section is valid for both paralleled systems, except when otherwise specified. Since the control principle is the same for each UPS, to avoid redundancy, only the schematic representation of UPS1 controller is demonstrated in Figure 4 as well as the variables sent from UPS1 controller to UPS2 controller and vice-versa. This figure also indicates the equations associated with the main stages of both UPS controllers: current references calculation, system state prediction at sample $k+1$ and $k+2$ as well as converter cost function minimization. Due to the reasons explained next, in Section 3.1, a delay of one sample is considered between signal measurement and control actions. As proposed in [23], a cooperative control strategy is adopted for both UPS systems. After measurements and model state prediction at $k+1$, the control action regarding the LSC is the first to be calculated. The LSC switching state is chosen having into account only its own effect in the system. However, to choose the switching state to apply on the DC-DC converter, the controller takes into account the switching state already chosen for the LSC. Similarly, to select the switching state to apply on the GSC, the controller takes into account the chosen switching state for LSC and DCC. The computed switching states are applied to the converters simultaneously with new signal measurements, beginning a new control cycle.

As it will be seen in Section 4, in the experimental implementation both UPS systems are controlled by the same control platform. However, the control algorithm was developed aiming to require as little communication as possible between the controllers, to ease the implementation in independent control platforms.

3.1. Controller Delay Compensation

In spite of the remarkable increase in processing capabilities of digital controllers, it is still impossible to acquire data, process it and output control decision almost instantaneously. Therefore, as used in [23,37,38], a delay of one sample is considered between signal measurement and the corresponding control action. All required signals are measured at k, and the system state is predicted at $k+1$ considering the previously chosen control action (applied at k). Finally the system state at $k+2$ is predicted for all possible switching states and the one that minimizes the cost function is selected and applied at $k+1$.

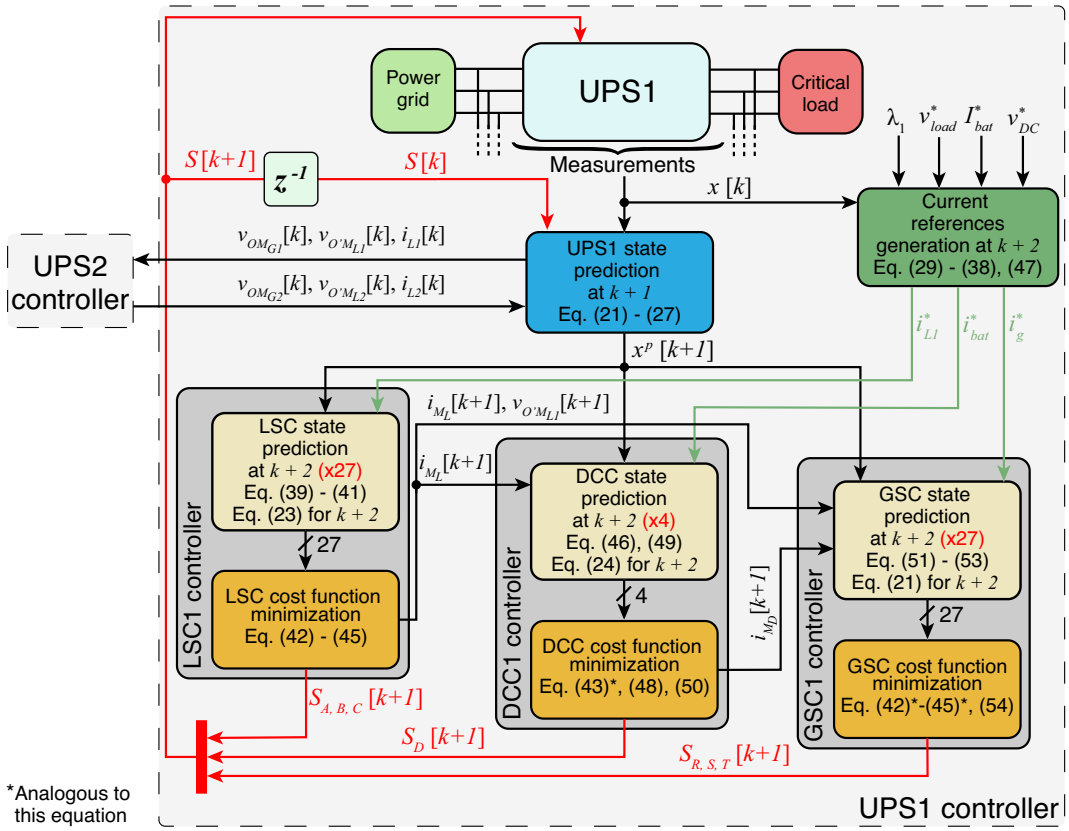

Figure 4. Schematic representation of the proposed UPS controller (UPS1).

Model prediction at $k+1$

In order to discretize the model, the forward Euler approximation is used. Hence, from (5), (6), (14), (17), (15) and (20) the following control variables at $k+1$ are respectively predicted:

$$\bar{i}_g^p[k+1] = \left(1 - \frac{R_G T_s}{L_G}\right)\bar{i}_g[k] + \frac{T_s}{L_G}\bar{v}_s[k] - \frac{T_s}{L_G}\bar{v}_g[k]\,, \tag{21}$$

$$v_{C_n}^p[k+1] = v_{C_n}[k] + \frac{T_s}{C_{DC}} i_{C_n}[k] \;\;,\;\; n = \{1,2\}\,, \tag{22}$$

$$\bar{i}_L^*[k+1] = \left(1 - \frac{R_L T_s}{L_L}\right)\bar{i}_L[k] - \frac{T_s}{L_L}\bar{v}_{load}[k] + \frac{T_s}{L_L}\bar{v}_L[k]\,, \tag{23}$$

$$i_{bat}^p[k+1] = i_{bat}[k] - \frac{R_D T_s}{L_D} i_{bat}[k] - \frac{T_s}{L_D} v_{bat}[k] + \frac{T_s}{L_D} v_D[k]\,, \tag{24}$$

$$\bar{v}_{load}^p[k+1] = \bar{v}_{load}[k] + \frac{T_s}{C_{eq}}(\bar{i}_{L_1}[k] + \bar{i}_{L_2}[k] - \bar{i}_{load_{(total)}}[k])\,, \tag{25}$$

$$i_0^p[k+1] = i_0[k] + T_s \cdot \frac{(v_{OM_{G2}} - v_{O'M_{L2}} + v_{O'M_{L1}} - v_{OM_{G1}})[k] - i_0[k] \cdot (R_{G_1} + R_{L_1} + R_{G_2} + R_{L_2})}{(L_{G_1} + L_{L_1} + L_{G_2} + L_{L_2})}\,, \tag{26}$$

where T_s is the control sampling time and C_{eq} is the equivalent load-side filter capacitor. For the prediction of the system state at $k+1$, each UPS system considers not only its own impact on the ZSCC, but also the impact of the state applied at k by the other UPS, in the form of the common mode voltage generated by the LSC and GSC. This improves the system state estimation and allows improved ZSCC

control, but requires communication between the two control platforms (of each UPS). However, the variables $v_{OM_{G1}}$ and $v_{O'M_{L1}}$ (or $v_{OM_{G2}}$ and $v_{O'M_{L2}}$) are computed within the previous sampling period, allowing this communication to start before the current sampling period begins. The load voltage prediction in (25) also requires each UPS controller to receive the LSC current values from the other UPS ($\bar{i}_{L_1}[k]$ and $\bar{i}_{L_2}[k]$). However, these values are measured directly and do not require any additional processing or calculations, so they can be transmitted immediately after sampling. Thus, the required communication should not pose a significant delay to the computation of the control algorithm.

The predicted grid voltage at $k+1$ is given by

$$\overline{v}_s^p[k+1] = \overline{v}_s[k] \cdot e^{j \cdot 2\pi \cdot f_g \cdot T_s}, \tag{27}$$

where f_g is the grid voltage frequency.

Over a sampling period, the battery voltage has a negligible variation. Thus, its predicted value at $k+1$ is equal to the measured voltage at sample k.

3.2. Load-Side Current References Calculation

Independently of the load power distribution between the paralleled systems, the generated load voltage must follow a sinusoidal voltage reference. Since a direct control of the load voltage does not allow a load-sharing strategy, this voltage is indirectly controlled through a control scheme based on direct current control. As proposed in [6], an equivalent output capacitor filter is defined as

$$C_{eq} = C_{L_1} + C_{L_2}. \tag{28}$$

The total current flowing in C_{eq} is controlled, so that the load voltage follows the generated voltage reference. The percentage of power that each system supplies to the load is defined by controlling the current that each system injects into C_{eq}. The proportion of load power assigned to UPS1 is defined as λ_1, whereby the proportion of power supplied by UPS2 is given by $\lambda_2 = 1 - \lambda_1$. Using the backward Euler approach, the total current necessary in the equivalent capacitor to track the output voltage reference is given by

$$\bar{i}^*_{L_{(total)}}[k+2] = \bar{i}_{load_{(total)}}[k+2] + \frac{C_{eq}}{T_s}\left(\overline{v}^*_{load}[k+2] - \overline{v}^p_{load}[k+1]\right), \tag{29}$$

where $\bar{i}^*_{L_{(total)}}[k+2]$ is the total reference current vector and $\overline{v}^*_{load}[k+2]$ is the sinusoidal reference voltage vector. The term $\bar{i}_{load_{(total)}}[k+2]$ corresponds to the total load current, which is directly measured by each UPS. Finally, the current references for each UPS system are obtained by multipling λ_1 and λ_2 by the total reference current $\bar{i}^*_{L_{(total)}}[k+2]$, respectively.

3.3. Grid-Side Current References Calculation

The developed control scheme for GSC control is similar to the one presented in [6,32]. However, in this work, for all the controllers instead of linear objective functions, quadratic objective functions are considered. This leads to a faster correction of large errors since a large error in a certain objective has a higher penalization. The grid current reference calculation is based on the active power balancing in each UPS. In order to get more stable grid currents, the average power is considered and not instantaneous power values. Thus, high variations in the load within a fundamental period are overlooked. Figure 5 shows the considered power flow directions in one UPS system.

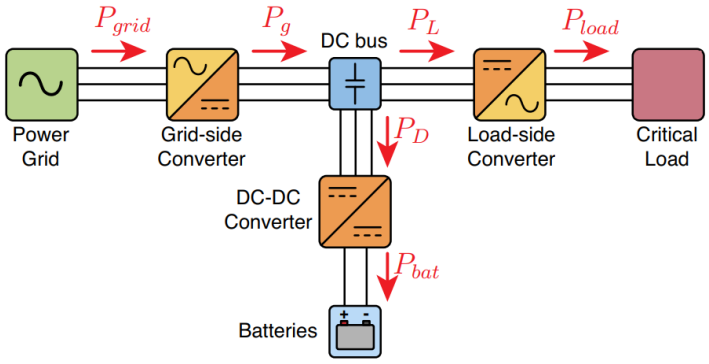

Figure 5. Power flow in a single UPS system.

The power balancing in one system can be written as

$$P^*_{grid} = (P_{grid} - P_g) + P_L + P^*_{charge} + (P^*_{bat} + (P_D - P_{bat})) \,, \tag{30}$$

where, P^*_{grid} corresponds to the reference active power to be drawn from the grid; P_{grid} is the power actually drawn from the grid; P_G is the power supplied by the grid-side converter to the DC bus; P_L is the power drawn from DC bus by the LSC; P_D is the power drawn from DC bus by the DCC. The difference $P_{grid} - P_g$ represents the losses in the GSC, whereas $P_D - P_{bat}$ represents the losses in the DCC. The term P^*_{charge} corresponds to the power necessary to charge/discharge the DC bus from its current voltage to its reference voltage. To obtain this term, the required energy to charge/discharge the capacitors needs to be calculated first using

$$E_{charge} = 2 \cdot \frac{1}{2} \cdot C_{DC} \cdot \left((\frac{v^*_{DC}}{2})^2 - (\frac{v_{DC}}{2})^2 \right) = \frac{1}{4} \cdot C_{DC} \cdot (v^{*2}_{DC} - v^2_{DC}) \,, \tag{31}$$

where C_{DC} represents the capacitance of one DC bus capacitor. The term v^*_{DC} is the DC bus voltage reference and v_{DC} is the measured bus voltage. The term P^*_{charge} is given by

$$P^*_{charge} = \frac{C_{DC} \cdot (v^{*2}_{DC} - v^2_{DC})}{4 \cdot T_s \cdot N_{th}} \,. \tag{32}$$

In order to limit the currents drawn by the GSC to charge/discharge the capacitors, a time horizon of Nth samples is considered. Thus, the controller always aims to charge/discharge the DC bus capacitors to the given voltage reference (v^*_{DC}) in Nth samples. Finally, the grid current references in the dq rotating frame are given by

$$i^*_{g_d} = \frac{2}{3} \frac{P^*_{grid}}{|\overline{v}_s|} \,, \tag{33}$$

$$i^*_{g_q} = \frac{2}{3} \frac{Q^*_{grid}}{|\overline{v}_s|} \,. \tag{34}$$

The amplitude and phase of grid voltage vector ($|\overline{v}_s|$ and $\angle\overline{v}_s$) are obtained using a Phase-Locked Loop (PLL). The term Q^*_{grid} is the target reactive power to be absorbed from grid. Usually, this term is desired to be null, however in specific cases, as for PF correction, it can be regulated into a certain value. To protect the GSC, it is critical that the reference currents do not surpass a maximum value, therefore the term $i^*_{g_{max}}$ was defined. To limit the dq calculated references a dynamic saturation process is adopted. Hence, the dq saturated current references are given by

$$i^*_{g_{d_{sat}}} = \begin{cases} i^*_{g_{max}} \cdot sign(|i^*_{g_d}|), & |i^*_{g_d}| > i_{g^*_{max}} \\ i^*_{g_d}, & otherwise \end{cases} \tag{35}$$

$$i^*_{g_{q_{sat}}} = \begin{cases} 0, & |i^*_{g_d}| > i_{g^*_{max}} \\ \sqrt{i^{*2}_{g_{max}} - i^{*2}_{g_d}}, & |i^*_{g_d}| \leqslant i^*_{g_{max}} \wedge |i^*_{g_d} + j \cdot i^*_{g_q}| > i_{g^*_{max}} \\ i^*_{g_q}, & otherwise \end{cases} \tag{36}$$

The dq saturated current references are transformed to $\alpha\beta$ components, using the following equation

$$\bar{i}^*_g[k+2] = i^*_{g_\alpha}[k+2] + j \cdot i^*_{g_\beta}[k+2] = (i^*_{g_{d_{sat}}} + j \cdot i^*_{g_{q_{sat}}}) \cdot e^{j(\angle \overline{v}_s + 2\pi f_{grid} \cdot 2T_s)} . \tag{37}$$

In order to obtain the references at $k+2$, the term $2\pi f_{grid} \cdot 2T_s$ is added to $\angle \overline{v}_s$.

During a situation where the GSC is not able to provide all the required active power, a part or the total value of this power must be supplied by the batteries through the DC-DC converter. Thus, the term P^*_{comp} is calculated by

$$P^*_{comp} = P^*_{grid} - P^*_{grid_{sat}} = P^*_{grid} - \frac{3}{2}(i_{g_{d_{sat}}} \cdot |\overline{v}_S|) . \tag{38}$$

When the grid voltage module ($|\overline{v}_S|$) drops bellow a predefined minimum threshold it is considered null by the controllers. In this case $P^*_{comp} = P^*_{grid}$ and all the power supplied to the load comes from the battery bank of the UPS.

3.4. Load-Side Controller

To minimize the required communication between each UPS system controller, the total reference current $i^*_{L_{(total)}}[k+2]$ is calculated in both controllers.

Objective function

The objective function defined for the LSC controller takes into account three objectives:

1. Converter output current vector error minimization;
2. Minimization of DC bus capacitors voltage unbalance;
3. Minimization of the ZSCC.

For the first objective, the predicted output converter current $\bar{i}^p_L[k+2]$ is calculated analogously to (23). In this equation $\overline{v}_L[k+1]$ corresponds to the converter voltage vector at $k+1$ and it is the only variable term in the equation, depending on the switching state being evaluated to be applied at sample $k+1$.

To achieve the second objective, the DC bus capacitors unbalance at $k+2$ is given by:

$$\Delta v^p_{C_{1,2}}[k+2] = \Delta v^p_{C_{1,2}}[k+1] + \frac{T_s}{C_{DC}} i_{M_L}[k+1] , \tag{39}$$

where $\Delta v^p_{C_{1,2}} = v^p_{C1} - v^p_{C2}$. The term $i_{M_L}[k+1]$ corresponds to the variable term in this equation.

As mentioned before, the proposed control strategy was developed aiming to require as little communication as possible between the controllers, to ease the implementation in independent control platforms. Hence, each UPS controller only knows the switching states to be applied at $k+1$ in the converters of the respective UPS. This avoids the need for each UPS controller to wait for signals computed by the remaining controllers within the same sampling period. Thus, to get the third objective, the predicted ZSCC considered by UPS1 and UPS2 controllers, when evaluating the control action for the respective LSCs are given by

$$i^p_{0_{L1}}[k+2] = i^p_0[k+1] + T_s \cdot \frac{v_{O'M_{L1}}[k+1] - i_0[k+1] \cdot (R_{G_1} + R_{L_1} + R_{G_2} + R_{L_2})}{(L_{G_1} + L_{L_1} + L_{G_2} + L_{L_2})} , \tag{40}$$

$$i^p_{0_{L2}}[k+2] = i^p_0[k+1] + T_s \cdot \frac{-v_{O'M_{L2}}[k+1] - i_0[k+1] \cdot (R_{G_1} + R_{L_1} + R_{G_2} + R_{L_2})}{(L_{G_1} + L_{L_1} + L_{G_2} + L_{L_2})}, \quad (41)$$

where $v_{O'M_{L1}}$ and $v_{O'M_{L2}}$ are the variable terms in the equations.

The partial objective functions regarding UPS output current, DC bus capacitors unbalance and ZSCC are respectively given by

$$g_{i_L} = (i^*_{L_\alpha}[k+2] - i^p_{L_\alpha}[k+2])^2 + (i^*_{L_\beta}[k+2] - i^p_{L_\beta}[k+2])^2, \quad (42)$$

$$g_{bal_L} = |v^p_{C1}[k+2] - v^p_{C2}[k+2]|^2, \quad (43)$$

$$g_{z_L} = |i^p_{0_L}[k+2]|^2. \quad (44)$$

The global objective function regarding LSC control is given by

$$G_{LSC} = g_{i_L} \cdot W_{i_L} + g_{bal_L} \cdot W_{bal_L} + g_{z_L} \cdot W_{z_L}. \quad (45)$$

As shown in Figure 6, this equation is evaluated for the 27 possible combinations, and combines partial objective functions g_x weighted by respective weights W_x, associated with each of the three objectives.

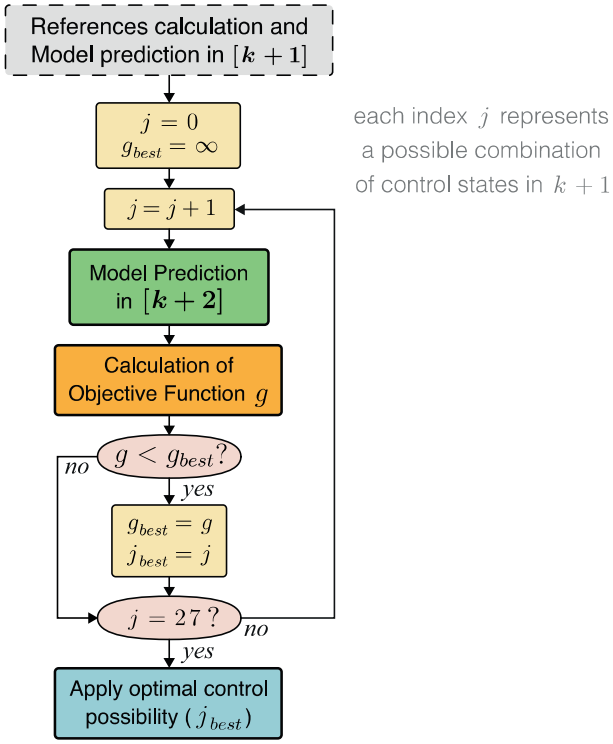

Figure 6. Flowchart regarding a cost function minimization.

3.5. DC-DC Controller

The controller regarding the DCC was implemented having as basis the conventional DC-DC converter controller proposed in [23]. Two objectives were defined for this controller:

1. Battery current reference tracking;
2. Minimization of the DC bus capacitor unbalance

Regarding the first objective, the battery current error at sample $k+2$ is given by

$$\Delta i_{bat}[k+2] = i^*_{bat}[k+2] - i^p_{bat}[k+2]\,. \tag{46}$$

The predicted battery current $i^p_{bat}[k+2]$ is calculated analogously to (24). In this case $v_D[k+1]$ corresponds to the variable term and is obtained from Table 2. The battery current reference is given by

$$i^*_{bat}[k+2] = I^*_{bat} - \frac{P^*_{comp}}{v_{bat}}\,, \tag{47}$$

where I^*_{bat} is the current reference to charge the batteries. Usually, this current comes from a battery management system, which was not studied in this work.

The partial objective function regarding the battery current is given by

$$g_{i_D} = |\Delta i_{bat}[k+2]|^2\,. \tag{48}$$

The predicted DC bus capacitors unbalance is given by

$$\Delta v^p_{C_{1,2}}[k+2] = \Delta v^p_{C_{1,2}}[k+1] + \frac{T_s}{C_{DC}}\left(i_{M_L}[k+1] + i_{M_D}[k+1]\right)\,, \tag{49}$$

where the term $i_{M_L}[k+1]$ is previously calculated in the LSC controller. By introducing this term in the DCC objective function, the effect of the LSC on the capacitors unbalance is taken into consideration in the DC-DC controller action. The partial objective function regarding capacitors unbalance g_{bal_D} is calculated analogously to (43).

Finally, the global objective function regarding the DC-DC controller is defined as

$$G_{DCC} = W_{i_D} \cdot g_{i_D} + W_{bal_D} \cdot g_{bal_D}\,. \tag{50}$$

This equation combines the partial objective functions with the respective weighting factors and is evaluated 4 times.

3.6. Grid-Side Controller

The switching state to be applied in the GSC is selected after the control actions taken for the LSC and DCC. Thus, to choose the optimal GSC action, each GSC controller receives information from the DCC and LSC controllers of the respective UPS.

Objective Function

Regarding the GSC control scheme, three objectives are also considered:

1. Reference grid current vector tracking;
2. Minimization of DC bus capacitors voltage unbalance;
3. Minimization of the ZSCC.

For the first objective, the predicted grid current vector $\vec{i}^{\,p}_g[k+2]$ is calculated analogously to (21).

For the second objective, the predicted DC bus capacitors unbalance is given by

$$\Delta v^p_{C_{1,2}}[k+2] = \Delta v^p_{C_{1,2}}[k+1] + \frac{T_s}{C_{DC}}\left(i_{M_L}[k+1] + i_{M_D}[k+1] - i_{M_G}[k+1]\right)\,, \tag{51}$$

where the terms $i_{M_L}[k+1]$ and $i_{M_D}[k+1]$ are previously calculated in the LSC and DCC controllers, respectively.

To achieve the third objective, the predicted ZSCC considered by each controller to select the control action for the GSCs is given by

$$i^{p}_{0_{G1}}[k+2] = i^{p}_{0}[k+1] + T_s \cdot \frac{v_{O'M_{L1}}[k+1] - v_{OM_{G1}}[k+1] - i_0[k+1] \cdot (R_{G_1} + R_{L_1} + R_{G_2} + R_{L_2})}{(L_{G_1} + L_{L_1} + L_{G_2} + L_{L_2})}\ , \quad (52)$$

$$i^{p}_{0_{G1}}[k+2] = i^{p}_{0}[k+1] + T_s \cdot \frac{v_{OM_{G2}}[k+1] - v_{O'M_{L2}}[k+1] - i_0[k+1] \cdot (R_{G_1} + R_{L_1} + R_{G_2} + R_{L_2})}{(L_{G_1} + L_{L_1} + L_{G_2} + L_{L_2})}\ . \quad (53)$$

In these equations, it can be seen that since the control action of each LSC was already selected, its effect is also taken into account in the respective GSC ($v_{O'M_{L1}}$,$v_{O'M_{L2}}$). Once again, each UPS controller considers only the CMV of its own converters.

Finally, the global objective function regarding GSC control is

$$G_{GSC} = g_{i_G} \cdot W_{i_G} + g_{bal_G} \cdot W_{bal_G} + g_{z_G} \cdot W_{z_G}\ . \quad (54)$$

where the terms g_{i_G}, g_{bal_G} and g_{z_G} are calculated analogously to (42)–(44), respectively.

4. Experimental Results and Discussion

In this section, experimental results are presented. The controllers are implemented in *Matlab/Simulink* environment and executed in a *dSpace MicroLabBox* control platform, which contains a dual-core PPC microprocessor and an FPGA. For controllers execution only the microprocessor was used, with the control algorithm of each UPS being assigned to a processor core. Two Yokogawa WT3000 power analyzers are used to monitor the power quality and the system efficiency. Figure 7 shows a schematic representation of the setup used for the experimental tests. Figure 8 shows a labeled picture of the experimental setup. A low-power prototype was used to experimentally demonstrate the effectiveness of the proposed control strategies.

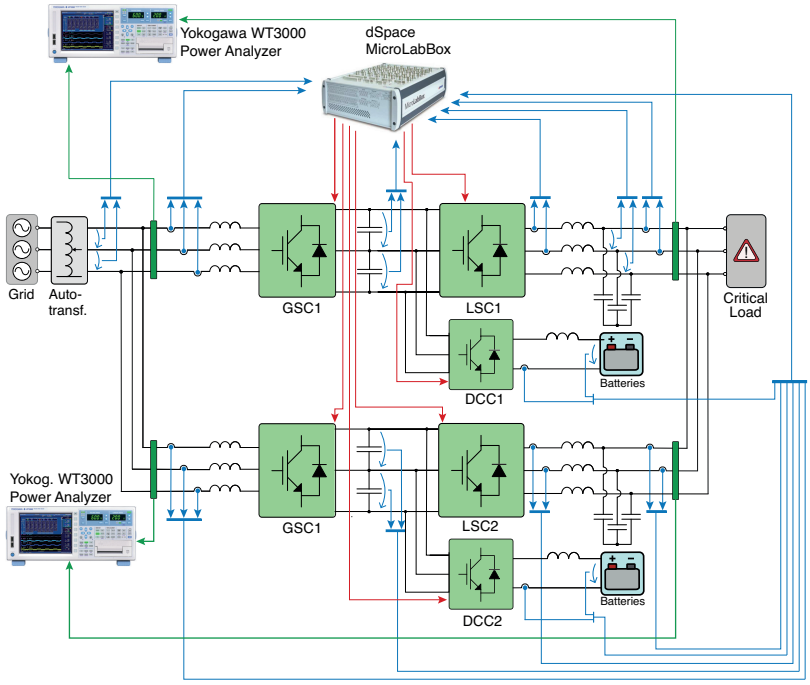

Figure 7. Schematic representation of the laboratory setup.

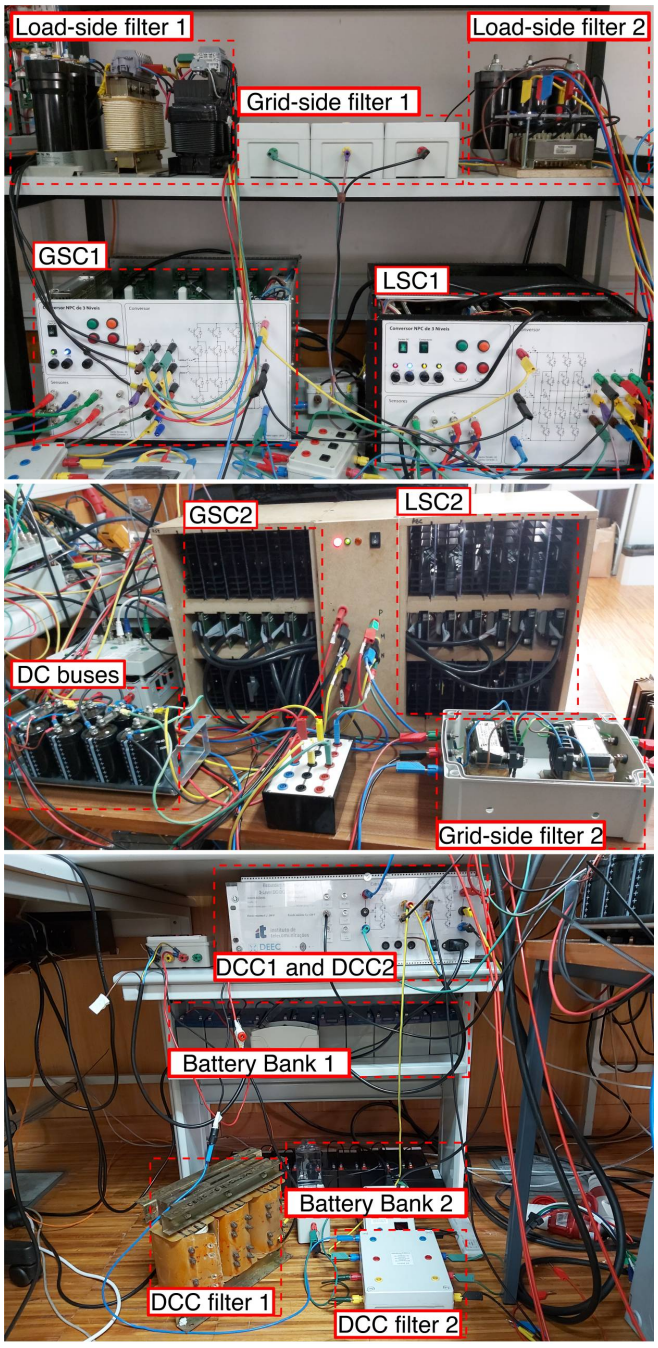

Figure 8. Experimental setup of the full system.

To protect the control platform, optical coupling was used for IGBTs activation. To choose the control sampling time, several experiments were made in order to select the minimum possible value, with which the control algorithm of both UPS systems can be executed without processor overrun occurring. Thus, from these experiments, a sampling time of 70 µs was selected. A highly non-linear load was used to demonstrate a correct system operation even in unfavorable load conditions, being one three-phase rectifier feeding an RC circuit (R= 33.3 Ω, C= 141 µF). The electrical parameters of the experimental tests are listed in Table 3. Different filter parameters were used in each UPS to prove the robustness of the proposed control methods in the parallel of asymmetric UPS systems. Each UPS battery bank consists of ten 12 V lead-acid batteries resulting in a battery bank voltage of approximately 120 V. The control references and weighting factors used in both UPS controllers are listed in Table 4.

These weighting factors were chosen through empirical tests and are used in the controllers of both UPS systems.

The presented results are organized as follows: firstly, given the asymmetries between systems, the individual performance of each UPS is demonstrated. Next, the parallel operation of the systems is presented. The effectiveness of the control strategy in suppressing the ZSCC is demonstrated. The merits of the proposed control schemes to distribute the load power between both systems under different load-sharing conditions is presented. An efficiency analysis is made demonstrating the importance of a fully controlled load power distribution. Then, the dynamic converters deactivation mechanism is presented. Finally, the simultaneous UPS systems commutation between normal and stored energy modes (grid failure/re-connection) is analyzed as well as the steady-state operation in stored energy mode.

Table 3. Electrical parameters.

Electrical Parameter	Value
Grid line voltage (RMS)	120 V
Grid voltage frequency	50 Hz
UPS1 grid-side filter	13.5 mH
UPS2 grid-side filter	5 mH
UPS1 DCC filter	11 mH
UPS2 DCC filter	14 mH
UPS1 and UPS2 DC bus capacit.	3 mF
LSC1 filter inductance	2.7 mH
LSC2 filter inductance	2 mH
LSC1 load-side filter capacitance	66 µF
LSC2 load-side filter capacitance	33 µF

Table 4. Control parameters.

Control Parameter	Value
Load line voltage (RMS)	120 V
Min. grid volt. module threshold	80 V
Load voltage frequency	50 Hz
DC charge horizon (N_{th})	500
Battery bank voltage 1 and 2	120 V
UPS1 and UPS2 DC bus volt. reference	220 V
W_{i_G}, W_{i_L}, W_{i_D}	1
W_{z_G} and W_{z_L}	3
W_{bal_G},W_{bal_D} and W_{bal_L}	0.3

4.1. Single UPS Operation

Given the asymmetry between the two UPS systems, a comparison between their individual performance feeding the load is presented in Figure 9.

In each case, the UPS that is providing power to the load is fully isolated from the other. This figure represents the grid voltage, the grid currents of each system, the DC bus capacitors voltage, the load voltage generated by each system and the currents after and before the load-side filters, respectively. It can be seen that due to its higher inductive grid-side filter, the UPS1 absorbs current with lower harmonic distortion than the UPS2, with a THD of 1.7% and 2.7%, respectively, as measured by each power analyzer.

Regarding the DC buses, it can be observed that the capacitors voltage balance is perfectly ensured in both systems. The mean voltage of each UPS2 DC bus capacitor is roughly 112 V, which leads to a DC bus voltage of approximately 224 V. This corresponds to a voltage error of 4 V ($\approx$ 1.82%). This steady-state error is caused by inaccuracies in the calculation of the powers absorbed/supplied by each DC bus. These inaccuracies are mainly imposed by delays in IGBTs activation, deviations

in the mathematical model and non-linearities in the circuit components. However, in terms of UPS performance the effect of these voltages deviations is negligible, and are therefore overlooked. The mean voltage of each UPS1 DC bus capacitor is approximately 109.5 V, presenting a lower steady state error than UPS2. Since the instantaneous power absorbed by the load has a non-linear behavior, a voltage ripple in the DC buses is observed. This could be avoided if an instantaneous power balancing was considered for the grid current references calculation. However, this approach would lead to highly distorted grid currents, which represents a much more undesirable situation.

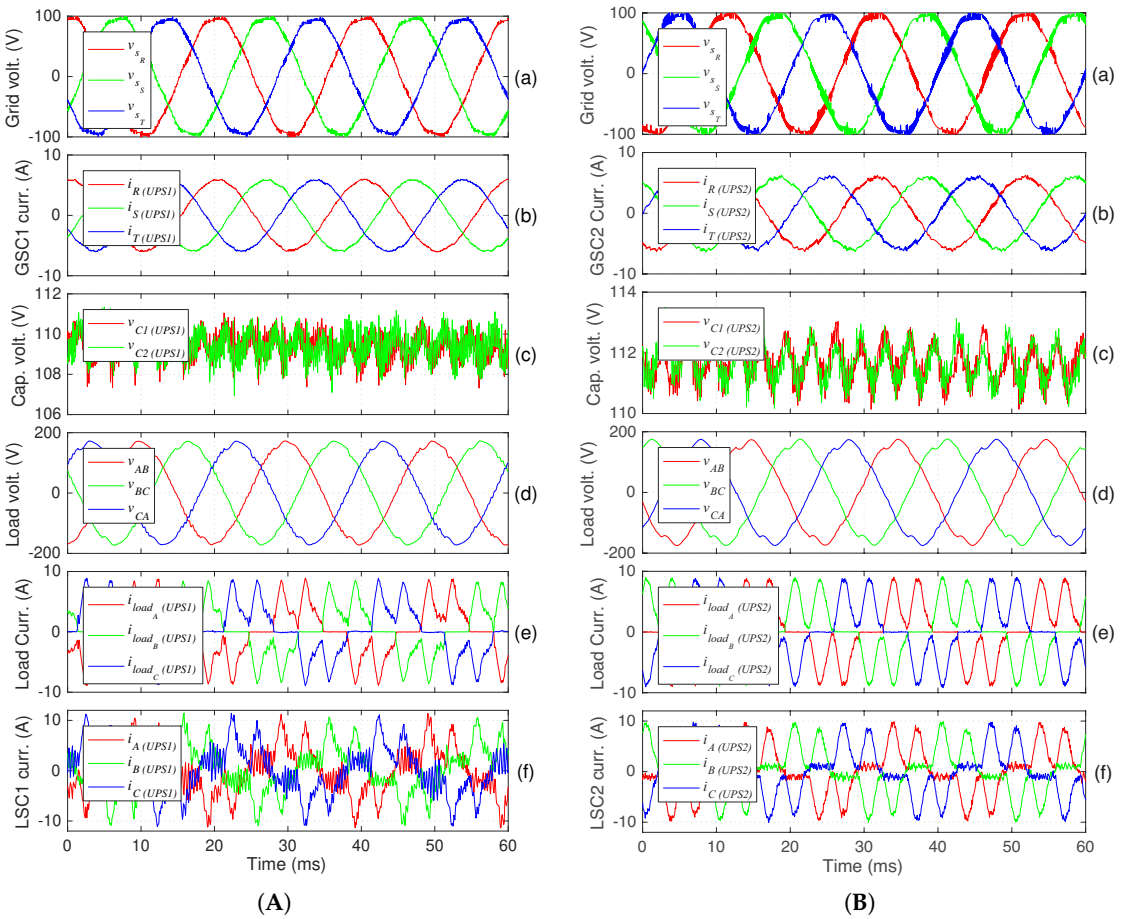

Figure 9. Individual UPS systems performance supplying the non-linear load: (**A**) UPS1 operation; (**B**) UPS2 operation.

As for the generated load voltage, due to a more inductive and capacitive filter, the UPS1 generates a voltage waveform with considerably lower harmonic distortion than the UPS2, with a THD of 2.5% and 4.9%, respectively.

These results demonstrate the considerably different behaviour of these two asymmetric UPS systems, which should make the control of the paralleled systems more complicated, with a well-defined power balance and ZSCC elimination being even more difficult to achieve. Despite this behaviour, the proposed control strategies are shown to correctly maintain all desired parameters as demonstrated by the following results.

4.2. Normal Mode

The parallel operation of both UPS systems, during normal mode is now addressed. These results intend to demonstrate the effectiveness of the proposed control strategy to eliminate the ZSCC and distribute power between the two UPS systems.

4.2.1. ZSCC Suppression

Figure 10 demonstrates the importance of eliminating the ZSCC as well as the effectiveness of the proposed control strategy in the suppression of this current. In this figure, the load voltage, the grid and the load currents (after the LC filters) of both UPSs as well as the ZSCC are represented. In this test, each UPS supplies half of the load power.

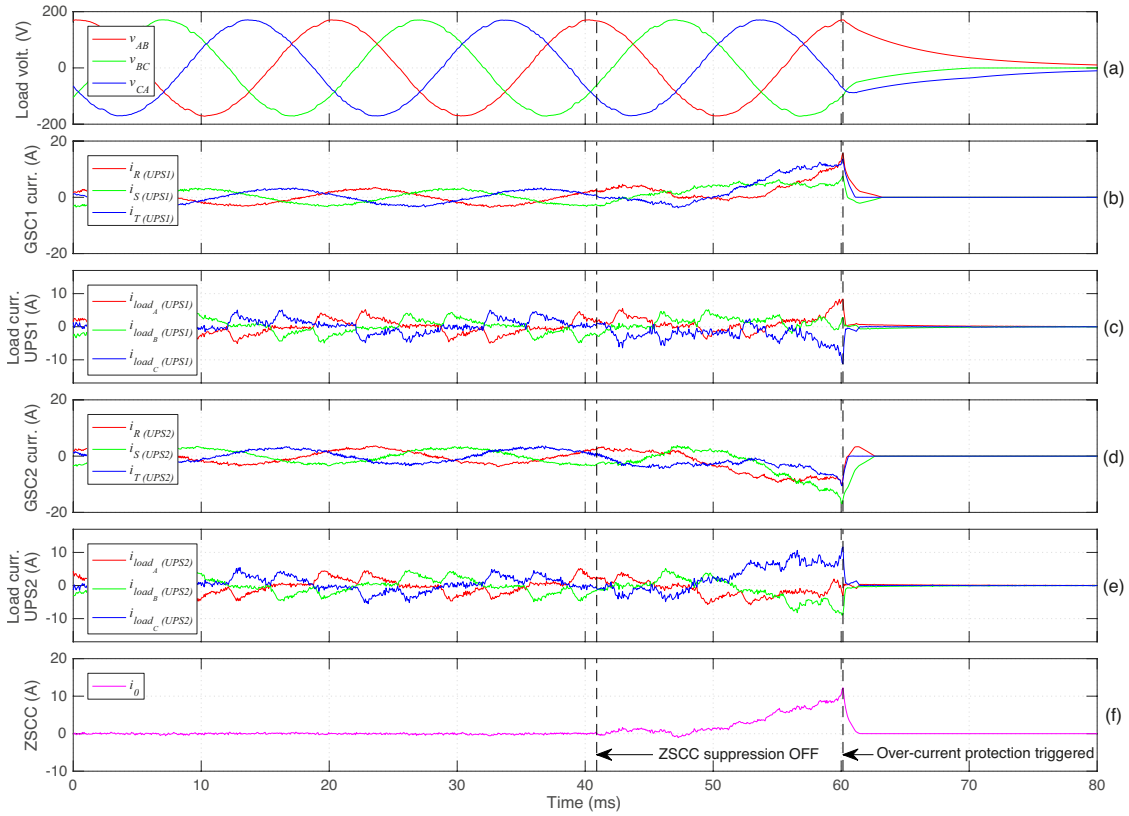

Figure 10. UPS systems performance during the deactivation of the ZSCC suppression: (**a**) Load Voltage; (**b**) UPS1 grid current; (**c**) UPS1 load current; (**d**) UPS2 grid current; (**e**) UPS2 load current; (**f**) Zero Sequence Circulating current.

Until $t = 42$ ms, the ZSCC suppression control is active ($W_{z_G} = W_{z_L} = 3$) and both UPS systems present a correct operation with near-sinusoidal grid currents waveforms (Figure 10b,d) as well as stable load currents (Figure 10c,e).

At $t = 42$ ms the ZSCC suppression is deactivated ($W_{z_G} = W_{z_L} = 0$). After this deactivation, a ZSCC immediately appears reaching a peak of approximately 10 A, after approximately 18 ms (Figure 10f). During this interval, the ZSCC highly distorts the phase currents of both systems and significantly increases their magnitude to levels that lead to higher electrical components stress and power losses, decreasing the overall system efficiency, as demonstrated in [32].

When the GSC1 grid current reaches 15 A ($t \approx 60$ ms), the corresponding overcurrent protection is triggered, because this value (15 A) is the predefined maximum admissible current at any point of the paralleled system. This grid current is roughly 3 times higher than the one that was observed while ZSCC suppression was active. To fully protect the prototype, when an over-current protection is triggered, all the converters are switched OFF, namely the LSCs. Thus, as Figure 10a shows, at $t \approx 60$ ms all power converters are deactivated and the load voltage is no longer ensured. These results clearly demonstrate the importance of eliminating the ZSCC as well as the effectiveness of the control scheme in its suppression.

4.2.2. Load-Sharing

The response of the system during power distribution changes is demonstrated in Figure 11.

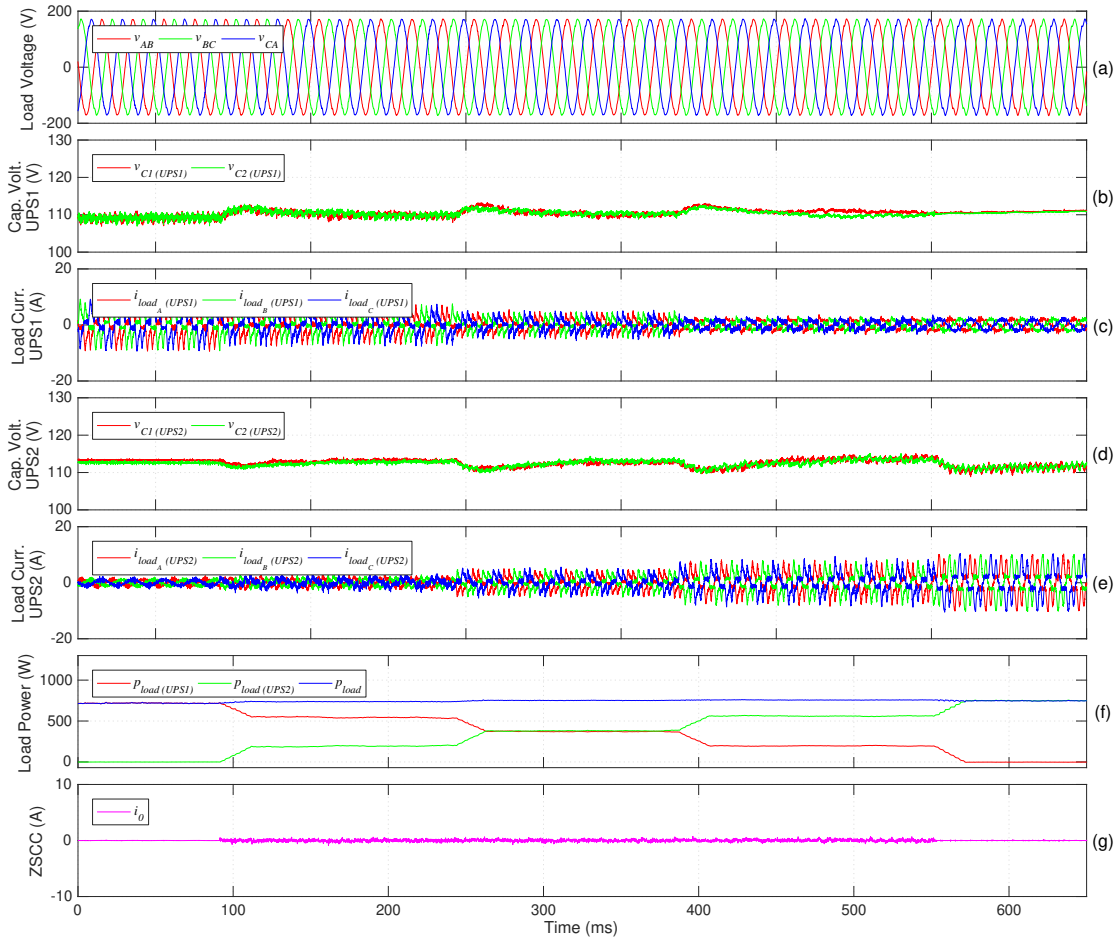

Figure 11. System performance when different percentage of the load power is assigned to each UPS: (**a**) Load Voltage; (**b**) DC bus capacitors voltage of UPS1; (**c**) UPS1 load current; (**d**) DC bus capacitors voltage of UPS2; (**e**) UPS2 load current; (**f**) Load power distribution and total load power; (**g**) Zero Sequence Circulating current.

This figure represents the load voltage, the DC buses capacitors voltage, the load currents of UPS1 and UPS2 and the ZSCC, respectively. At the beginning of this test, UPS1 is providing all the load power. Since UPS2 supplies no power, the IGBTs of UPS1 are all switched OFF (the need for this deactivation will be demonstrated later). Then, the percentage of load power supplied by UPS2 is sequentially incremented by 25% until it supplies the total load power.

It can be seen from Figure 11a that a high-quality output voltage waveform is permanently ensured by the paralleled systems for different load-sharing conditions. From the output currents (Figure 11c,e) it is observed that the power supplied by each UPS changes almost immediately to the target value. A slower transition is observed in the output average power (Figure 11f) simply because a time horizon of one period is considered in its calculation, so it takes a full period to stabilize at the new value. When the percentage of the load power assigned to a UPS is set to zero, a load-side current is observed in the corresponding UPS. However, this current corresponds to an almost purely reactive current that circulates through the capacitors of the respective load-side filter.

During these fast power distribution changes, the DC bus capacitors voltage balance of both UPS systems (Figure 11b,d) is completely ensured. When a UPS does not provide power to the load ($\lambda_1 = 0$ or $\lambda_2 = 0$) a DC bus voltage increase may occur. Since the inputs/outputs terminals of both UPS are

still physically connected, if the grid and load voltage are not synchronized, the voltage established between the inputs and output can actually charge the capacitors with a higher voltage. The worst case (grid and load voltage in phase-opposition) could lead to a peak voltage of two times the peak of the grid/load voltage being applied to the DC bus, which could be dangerous to the system. Hence, to avoid this problem in industrial applications, the load voltage references should be generated using the grid voltage phase given by the PLL that is synchronized with the grid.

From Figure 11g it is possible to see that the ZSCC is practically zero with any load-sharing condition, which is crucial for the stable operation of both systems. When the percentage of the load power assigned to a UPS is zero, its IGBTs are switched off (this operation option will be explained later). In this case no path exists for the ZSCC circulation, leading to a null value. During the other load-sharing conditions ($\lambda_1 \neq 0$ and $\lambda_2 \neq 0$), in which both UPS systems are operating, a ZSCC can circulate so it is not exactly zero. However, it is kept at very low levels by the controllers, appearing as a small ripple around zero.

Figure 12 shows the power analyzer results that demonstrate relevant measures when the non-linear load is equally shared by the two UPS systems ($\lambda_1 = \lambda_2 = 0.5$).

(**a**) (**b**)

Figure 12. Power analyzer results when the systems are equally sharing the non-linear load: (**a**) UPS1 providing 50% of the load power; (**b**) UPS2 providing 50% of the load power.

Two grid-side and two load-side voltage and current wave-forms are measured by the respective analyzer. According to these results, the UPS1 is absorbing approximately 458.95 W from the grid (parameter P∑A), whereas UPS2 is absorbing 453.95 W. Both UPS are absorbing power with approximately unit power factor (≈ 0.99). Each UPS provides approximately 381.7 W and 380.2 W to the load ($P\sum B$), which demonstrates the high obtained load-sharing precision, even for asymmetric systems. An efficiency of about 83.17% (parameter η_1) and 83.75% is obtained in UPS1 and UPS2, respectively. Thus, for the same provided load power, a higher efficiency is obtained in the system with lower grid-side and load-side filter parameters. The overall system efficiency is 83.46%. The THD of the grid-side currents of the UPS1 and UPS2 are 4.64% and 6.54% (*Ithd2*), respectively. However, since the ZSCC circulates exclusively through the paralleled UPS systems, the total grid currents (effectively drawn from the power grid) present low distortion ($\approx 2\%$). These two THD current values (4.64% and 6.54%) are considerably higher because of the remaining ZSCC current ripple around zero (shown in Figure 11g). Almost no ripple is observed in the first grid voltage and current wave-forms (*U1* and *I1*) provided by each Power Analyzer just because a low-pass line filter (internal to the power analyzer, cutoff frequency = 500 Hz) has to be active to provide stable PLL response and measurements. As seen in Figure 12, regarding the load line voltage, both power analyzers indicate a RMS value of approximately 121 V (*Urms3*), with a THD value around 1.4% (*Uthd3*).

The performance of the UPS systems during asymmetric power distribution is demonstrated in Figure 13. In this test, UPS1 is supplying 25% of the load power, whereas UPS2 is providing the remaining 75% of the power to the load.

(**a**) (**b**)

Figure 13. Power analyzers results during asymmetric load-sharing: (**a**) UPS1 providing 25% of the load power; (**b**) UPS2 providing 75% of the load power.

According to the Yokogawa Power Analyzers, the values for active power absorbed by UPS1 and UPS2 are 251.9 W and 666.7 W, respectively. Both UPS systems absorb power with high power factor ($\approx$ 0.99 for UPS1 and UPS2). Each system provides approximately 201.6 W and 557 W to the non-linear load. Efficiency values of approximately 80.02% (η_1) and 83.55% are obtained to UPS1 and UPS2 systems, respectively. The overall efficiency is approximately 82.58%. These results demonstrate that different load power distributions lead to different system efficiencies, which allows to manage the efficiency of both systems and consequently the overall system efficiency. Hence, a perfectly defined load-sharing control can enable an optimization of the overall system efficiency. The THD values of the grid-side currents of both UPS systems are 6.38% and 3.91%, respectively. Finally, it is possible to observe that even with an asymmetric sharing of a non-linear load current, high-quality load voltage waveforms are obtained with RMS value of approximately 121.3 V and THD value of roughly 1.9%.

4.2.3. Efficiency Analysis

Table 5 presents the powers managed by each UPS with different load-sharing conditions, as well as the individual and overall system efficiencies, measured with the Yokogawa WT3000 power analyzers. To clearly show the importance that an asymmetric load power distribution can have in terms of efficiency, a lower power load is connected to the paralleled system. For the results presented in this section, a 100 Ω resistor was used in the load, instead of the 33.3 Ω resistor used in the remaining tests.

Table 5. Powers (W) and efficiencies (%) when the non-linear load is supplied.

λ_1	λ_2	$P_{grid_{(1)}}$	$P_{load_{(1)}}$	η_1	$P_{grid_{(2)}}$	$P_{load_{(2)}}$	η_2	$P_{grid_{Total}}$	$P_{load_{Total}}$	η_{Total}
0	1	-	-	-	334	272	81.44	334	272	81.44
0.25	0.75	95	63	66.32	263	208	79.09	358	271	75.70
0.5	0.5	176	132	75	172	135	78.49	348	267	76.72
0.75	0.25	284	217	76.41	83	55	66.27	367	272	74.11
1	0	339	266	78.47	-	-	-	339	266	78.47

In this test, UPS2 starts by supplying the total load power. Then, the percentage of the load power supplied by UPS1 is sequentially incremented by 25% until it supplies the entire load power ($\lambda_1 = 1$ and $\lambda_2 = 0$).

During these power distribution changes, the power absorbed by UPS1 system $P_{grid_{(1)}}$ varies between 0 and 339 W, whereas the power supplied to the load $P_{load_{(1)}}$ goes from 0 to 266 W. The efficiency of this system presents its maximum for $\lambda_1 = 1$, which corresponds to the case that the system provides the full load power ($\eta_1 = 78.47\%$). As for UPS2, the absorbed power $P_{grid_{(2)}}$ varies between 334 and 0 W, whereas its output power $P_{load_{(2)}}$ goes from 272 to 0 W. Similarly to UPS1, its maximum efficiency ($\eta_2 = 81.44\%$) is observed for $\lambda_2 = 1$. These results clearly show that the efficiency of a given UPS system changes with the load.

It is also clear that the overall system efficiency depends on the power distribution. In this particular case, higher efficiency values are obtained when a single UPS is providing 100% of the load power ($\eta_{Total} = 78.47\%$ and $\eta_{Total} = 81.44\%$). The highest overall efficiency ($\eta_{Total} = 81.44\%$) is achieved when UPS2 supplies the total load power, due to its lower filter parameters. Regarding the other load-sharing conditions ($\lambda_1 \neq 0$ and $\lambda_2 \neq 0$), the highest overall efficiency value ($\eta_{Total} = 76.72\%$) is obtained for a 50%/50% distribution. Nevertheless, this is a significantly lower value compared to the overall efficiency obtained when UPS2 supplies the total load power (81.44%).

These results clearly demonstrate that a fully controlled load power distribution can be highly advantageous, since it enables the possibility of efficiency improvement strategies to be implemented.

4.3. Converters Deactivation Mechanism

The importance of the proposed deactivation mechanism is demonstrated in Figure 14.

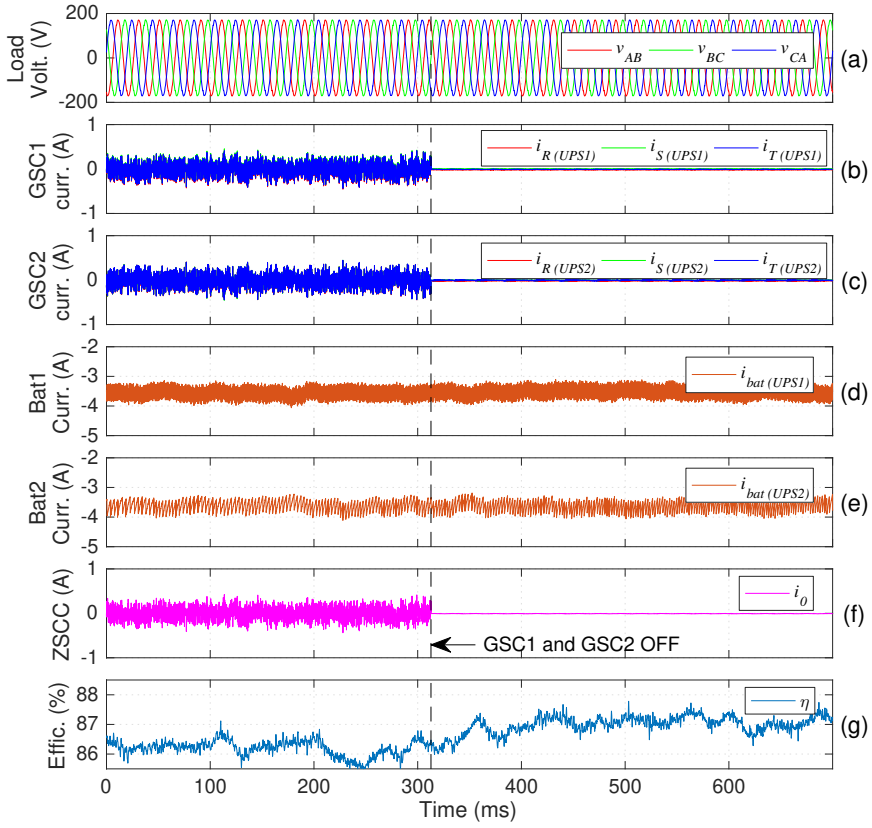

Figure 14. Impact of GSC pulses deactivation in system efficiency during stored energy mode: (**a**) Load Voltage; **(b)** UPS1 grid currents; (**c**) UPS2 grid currents; (**d**) UPS1 battery current; (**e**) UPS2 battery current; (**f**) Zero Sequence Circulating Current; (**g**) Global system efficiency.

This figure represents the load voltage, the grid and battery currents of each UPS, the ZSCC and the overall system efficiency, respectively. Both UPS systems operate in stored energy mode, which means that the load power comes from the battery banks of each UPS. In this test, the IGBTs of the GSCs were kept active until $t = 313$ ms, and at that instant, they are switched OFF. As Figure 14a shows, the load voltage waveform is not affected by the deactivation of the GSCs.

When the GSCs are active, paths for the circulation of the ZSCC are formed. On the other hand, when they are deactivated, since all their power switches are left in open circuit, the GSC currents are null (Figure 14b,c) and no possible paths for the ZSCC exist (Figure 14f). When the GSCs controllers are active, the switching state '0' is being continuously selected by the GSC1 and GSC2 controllers for all the legs of the GSCs ($S_R = S_S = S_T = 0$). With such switching states applied, the contribution of the GSC1 and GSC2 to the dynamics of the ZSCC is actually null, but a path for ZSCC exists. Thus, only the switching states chosen by the LSCs lead to the creation of the ZSCC. Until the GSCs deactivation, the controllers of the LSCs are controlling the ZSCC, keeping this current oscillating around zero, as seen in Figure 14f. With the GSCs active, the ZSCC is not exactly zero and it clearly exceeds peaks of 0.5 A. The circulation of this current through the grid-side filters and the conduction losses in GSC1 and GSC2 introduce additional active power loses in the overall system. As aforementioned, when the GSCs are OFF, no paths for the ZSCC exist, and this current is null. Hence, the power losses are reduced and as shown in Figure 14g the global system efficiency increases around 1%. This clearly shows the advantages of fully disabling the GSCs when the grid is unavailable, demonstrating the need for the proposed converter deactivation mechanism.

A similar situation is observed when a given UPS should supply no power ($\lambda_1 = 0$ or $\lambda_2 = 0$). If the converters remain enabled, with zero-references, a ZSCC can circulate and the overall system efficiency is reduced. On the other hand, if the unused UPS is disabled, the ZSCC is completely eliminated and the overall efficiency is improved.

The deactivation of the IGBTs of converters "unnecessary" for a given operation condition eliminates any possible path for the ZSCC circulation. This decreases the overall power losses and increases the overall system efficiency. Moreover, with this technique the IGBTs lifetime can be extended.

4.4. Stored Energy Mode and Commutation between Modes

To detect a grid failure/re-connection, each UPS controller compares the grid voltage module given by the respective PLL, with a predefined minimum threshold which is equal for both UPS systems. Figures 15 and 16 show the system response to the failure and re-connection of the power grid, respectively.

Figure 15 demonstrates two relevant situations: the transient response after the grid failure and the operation in stored energy mode (load fed from the batteries). In this test, each UPS supplies 50% of the total power absorbed by the non-linear load. Until the grid failure, each UPS system operates in normal mode, with power flowing from the power grid to the load through the GSC and LSC of each UPS. As observed in Figure 15a, the grid failure generates a voltage transient, until the grid currents of both UPS systems reach zero (Figure 15c,d, respectively). The response of the UPS controllers is not immediate, since both PLLs take some time to detect the change (Figure 15b). Shortly after the grid currents of both UPS are extinguished, the PLLs simultaneously detect the interruption of the grid voltage. The grid-side converters are deactivated and the DC-DC converters start to supply the required power to the DC buses, discharging the batteries. In this condition, the batteries of UPS1 and UPS2 supply a current of approximately 3.5 A as observed in Figure 15e,f, respectively. During the discharge, a decrease in the battery bank voltage of UPS1 and UPS2 is observed, visible in Figure 15g,h, respectively. The grid failure has little impact on DC bus of both UPS systems, with the DC buses having a small voltage drop which is quickly compensated as visible in Figure 15i,j. This voltage drop happens due to the fact that the current references are not instantaneously updated, since they are calculated considering a grid voltage period. Through these two sub-figures, it is also observed

that the DC buses capacitors voltage remain perfectly balanced. No deterioration in the load voltage waveform is verified during and after the transient between the two modes of operation, as visible in Figure 15k. Throughout these operation modes the THD of the load voltage is approximately 1.4%. As it can be seen in Figure 15l, the defined load power distribution remains constant with each UPS supplying approximately 50% of the load power.

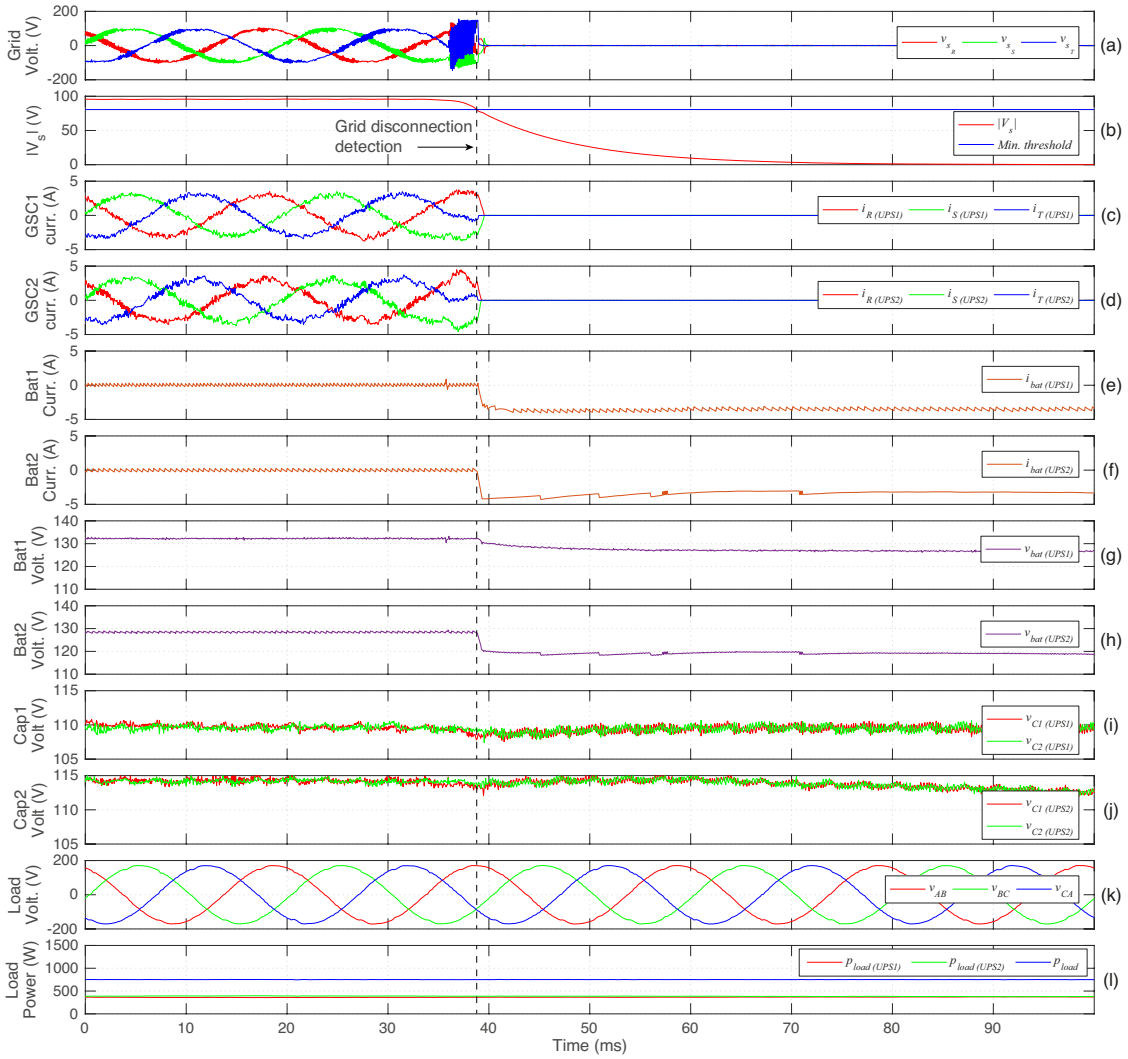

Figure 15. UPSs performance during grid disconnection: (**a**) Grid Voltage; (**b**) Grid voltage module; (**c**) UPS1 grid currents; (**d**) UPS2 grid currents; (**e**) UPS1 battery current; (**f**) UPS2 battery current; (**g**) UPS1 battery bank voltage; (**h**) UPS2 battery bank voltage; (**i**) DC bus capacitors voltage of UPS1; (**j**) DC bus capacitors voltage of UPS2; (**k**) Load Voltage; (**l**) Load power distribution and total load power.

Figure 16 shows the system response when the power grid is re-connected to the system. The measured signals represented in this figure are the same of Figure 15.

After the grid re-connection, the PLLs take roughly 100 ms to detect the presence of the grid and about 30 ms to perfectly synchronize with the grid voltage, creating a short period in which slightly larger grid currents are generated. After PLLs stabilization, stable currents are generated by both GSC controllers and the global UPS system starts working in normal operation with the currents supplied by the DC-DC converters being zero. No disturbance in the load voltage waveform is verified during the transient between these two modes of operation. During and after the re-connection, the load-sharing condition is kept, with each UPS supplying 50% of the load power.

These results demonstrate the good performance of the proposed control system, with seamless transitions between UPS operation modes and good steady-state performance in both normal and stored energy modes. The UPS guarantees a good quality load voltage waveform regardless of the operation mode, as well as an effective ZSCC suppression and load power distribution.

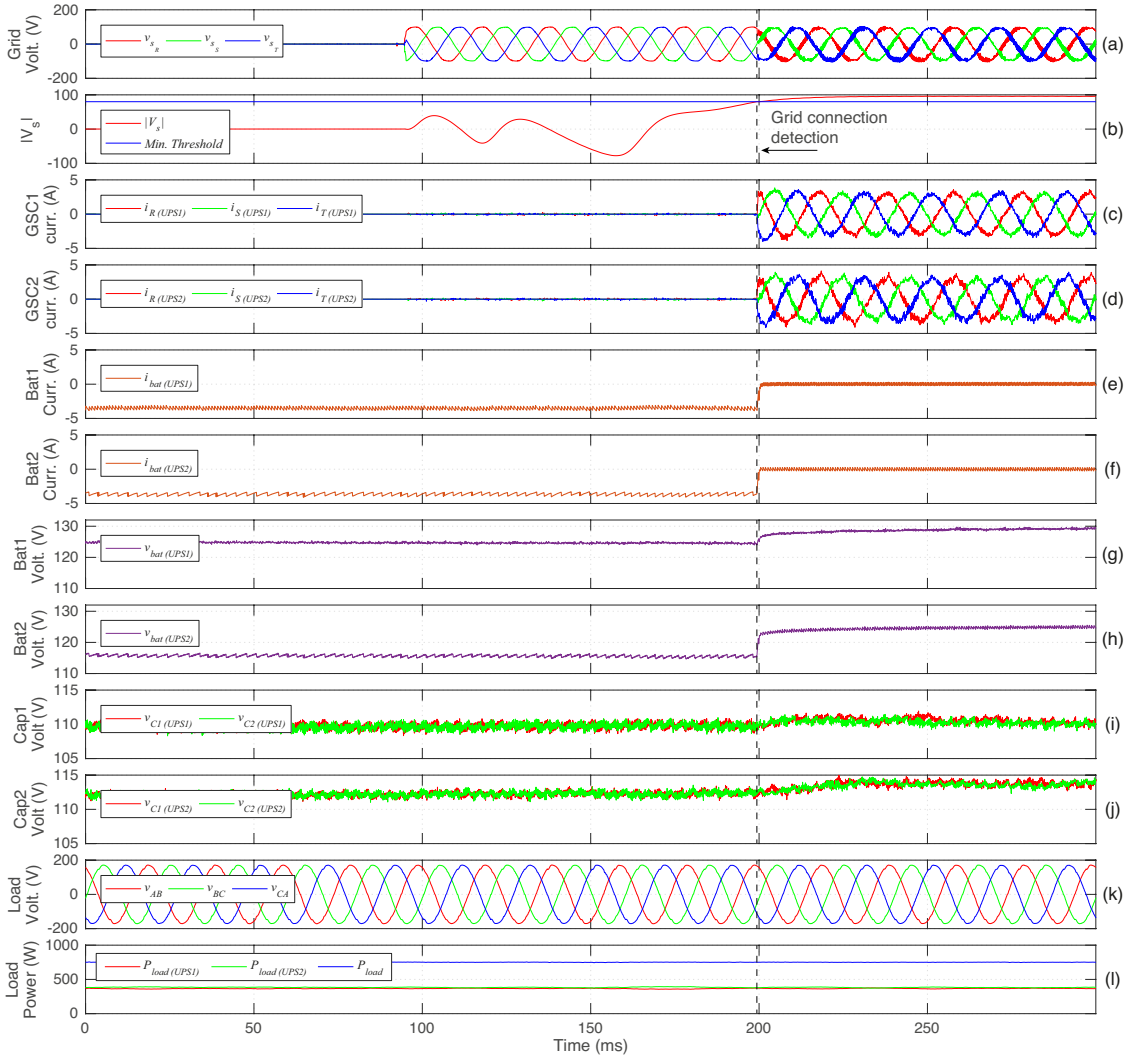

Figure 16. UPSs performance during grid connection: (**a**) Grid Voltage; (**b**) Grid voltage module; (**c**) UPS1 grid currents; (**d**) UPS2 grid currents; (**e**) UPS1 battery current; (**f**) UPS2 battery current; (**g**) UPS1 battery bank voltage; (**h**) UPS2 battery bank voltage; (**i**) DC bus capacitors voltage of UPS1; (**j**) DC bus capacitors voltage of UPS2; (**k**) Load Voltage; (**l**) Load power distribution and total load power.

5. Conclusions

In this paper, the parallel operation of two multilevel double conversion Uninterruptible Power Supply (UPS) systems is studied.

The zero sequence circulating current (ZSCC) that circulates between both UPS systems is analyzed. The dynamics of this current depends on a linear combination of the common mode voltages (CMVs) generated by the grid-side converters (GSC) and load-side converters (LSC). By controlling the CMV generated by these converters, the ZSCC can be suppressed.

The proposed finite control set model predictive control (FCS-MPC) strategies demonstrates high performance, even when two asymmetric UPS systems are used. During normal operation, the circulating current is effectively suppressed and a fully controlled load-sharing (symmetric or asymmetric) is obtained, with a high-quality voltage waveform being permanently ensured.

As demonstrated by the presented efficiency analysis, the controlled load-sharing provided by the proposed technique can be used to improve the overall system efficiency.

A power converter deactivation technique is also proposed. With such technique, according to the operation mode, each converter is deactivated when it is not needed (when the grid is unavailable or when a UPS is instructed to supply no power to the load). This eliminates any ZSCC circulation path and reduces the power losses in the system, increasing the overall system efficiency. Moreover, with this solution, the power switch lifetime can be extended.

Finally, the presented results demonstrate that the proposed UPS system provides good dynamic response during grid failure/re-connection (transition between operating modes). The two UPS systems perfectly maintain the defined load-sharing condition as well as a high-quality voltage waveform, even during the transient.

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